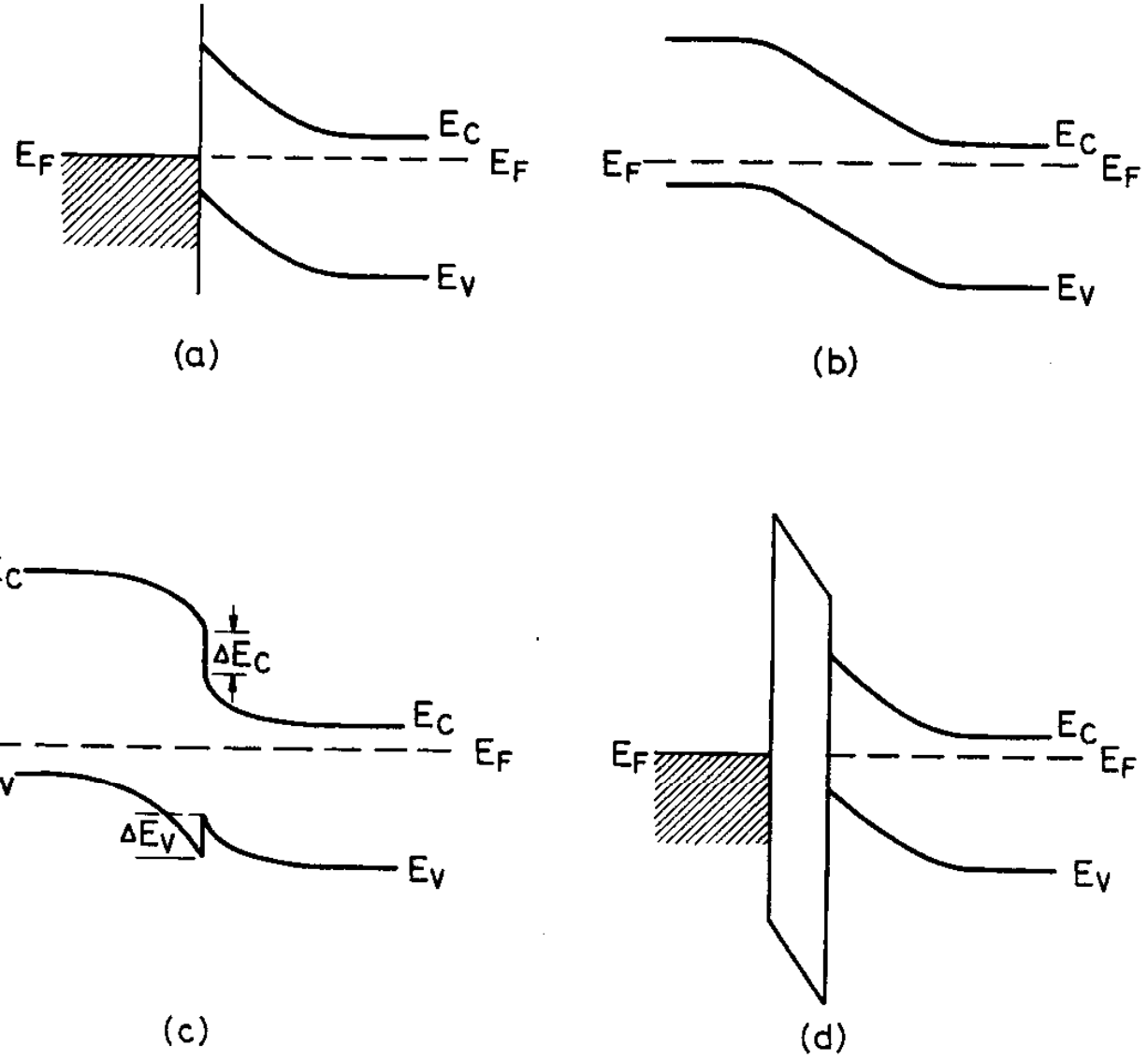
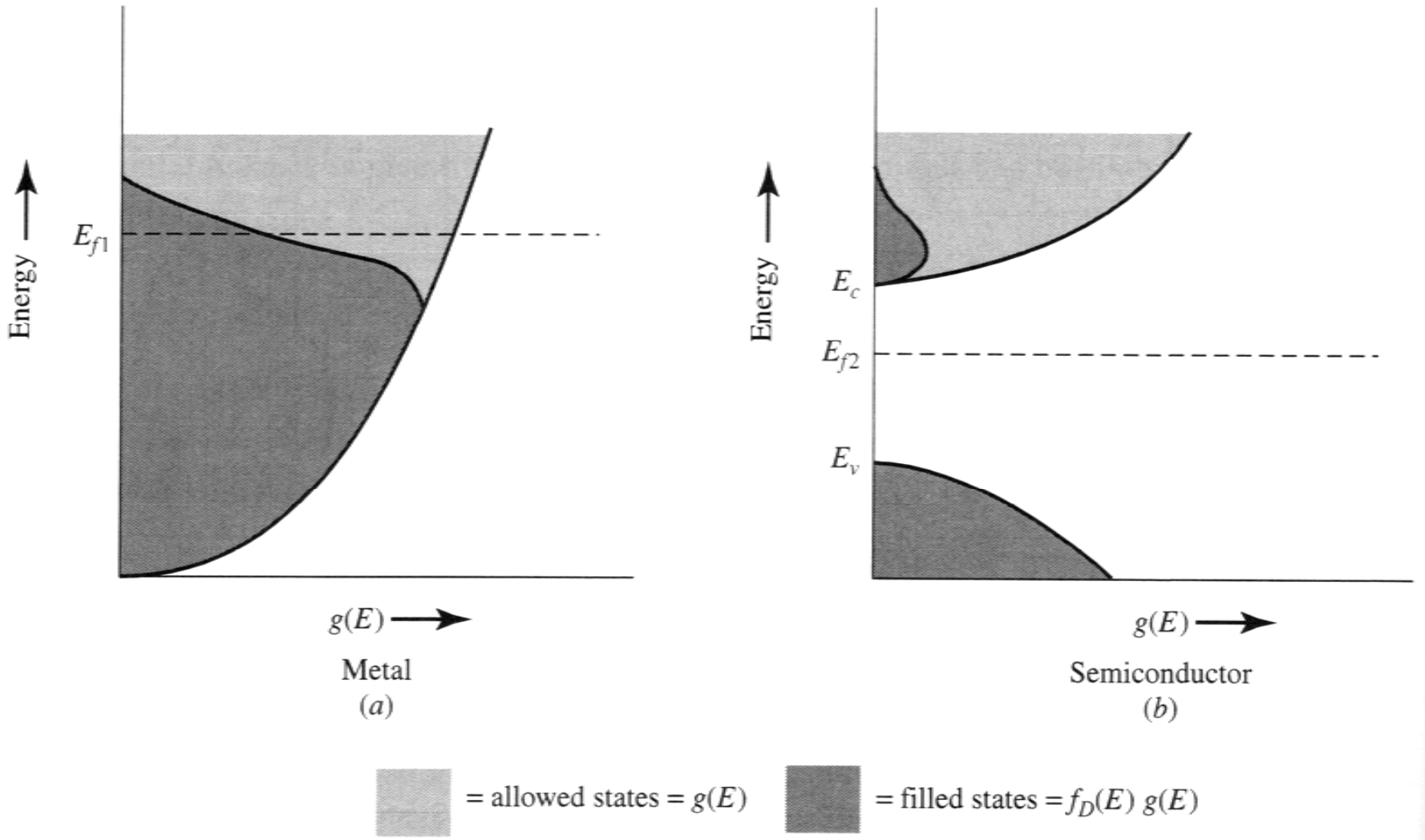
Metal-Semiconductor Interfaces

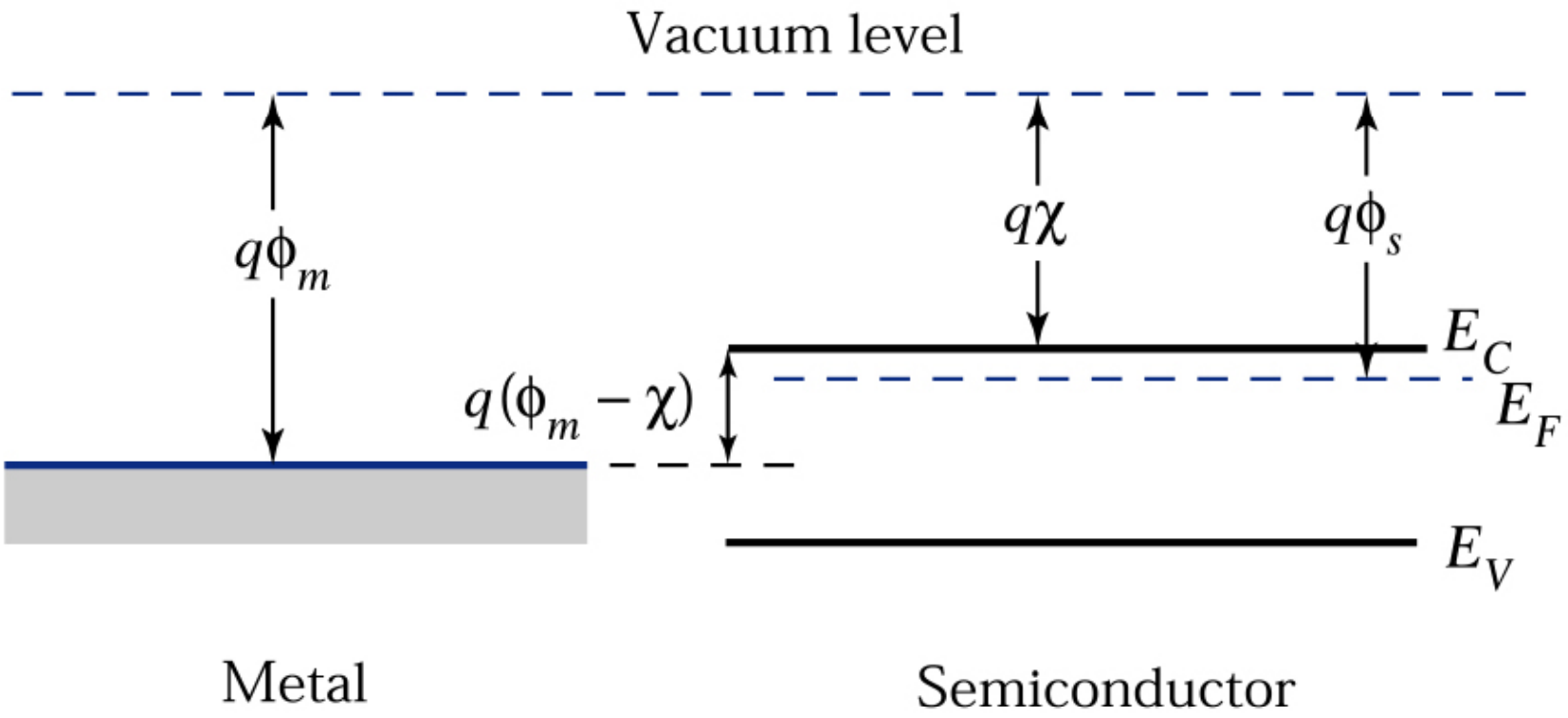
- **Metal-Semiconductor contact**
- **Schottky Barrier/Diode**
- **Ohmic Contacts**
- **MESFET**

Device Building Blocks

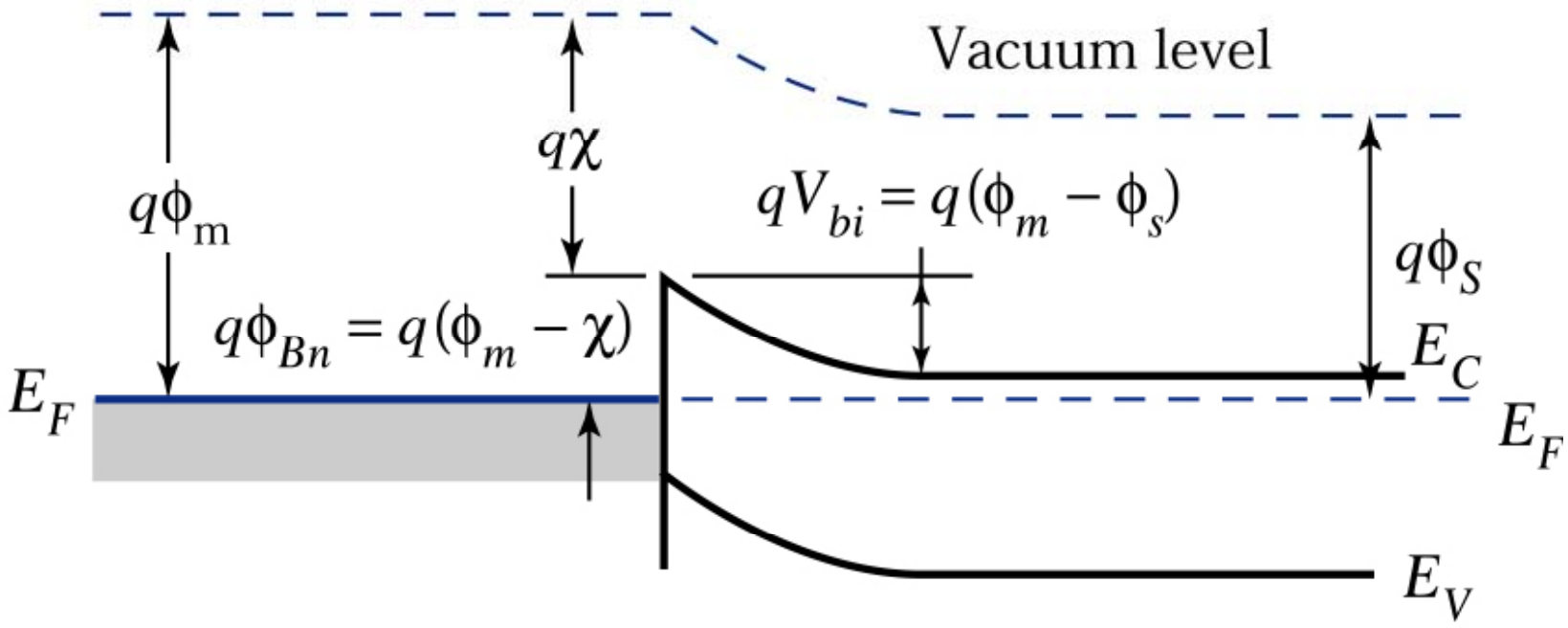



Energy
E_{f1}
$g(E)$
Metal
(a)
Energy
E_c
E_{f2}
E_v
$g(E)$
Semiconductor
(b)
= allowed states = $g(E)$
= filled states = $f_D(E)\ g(E)$

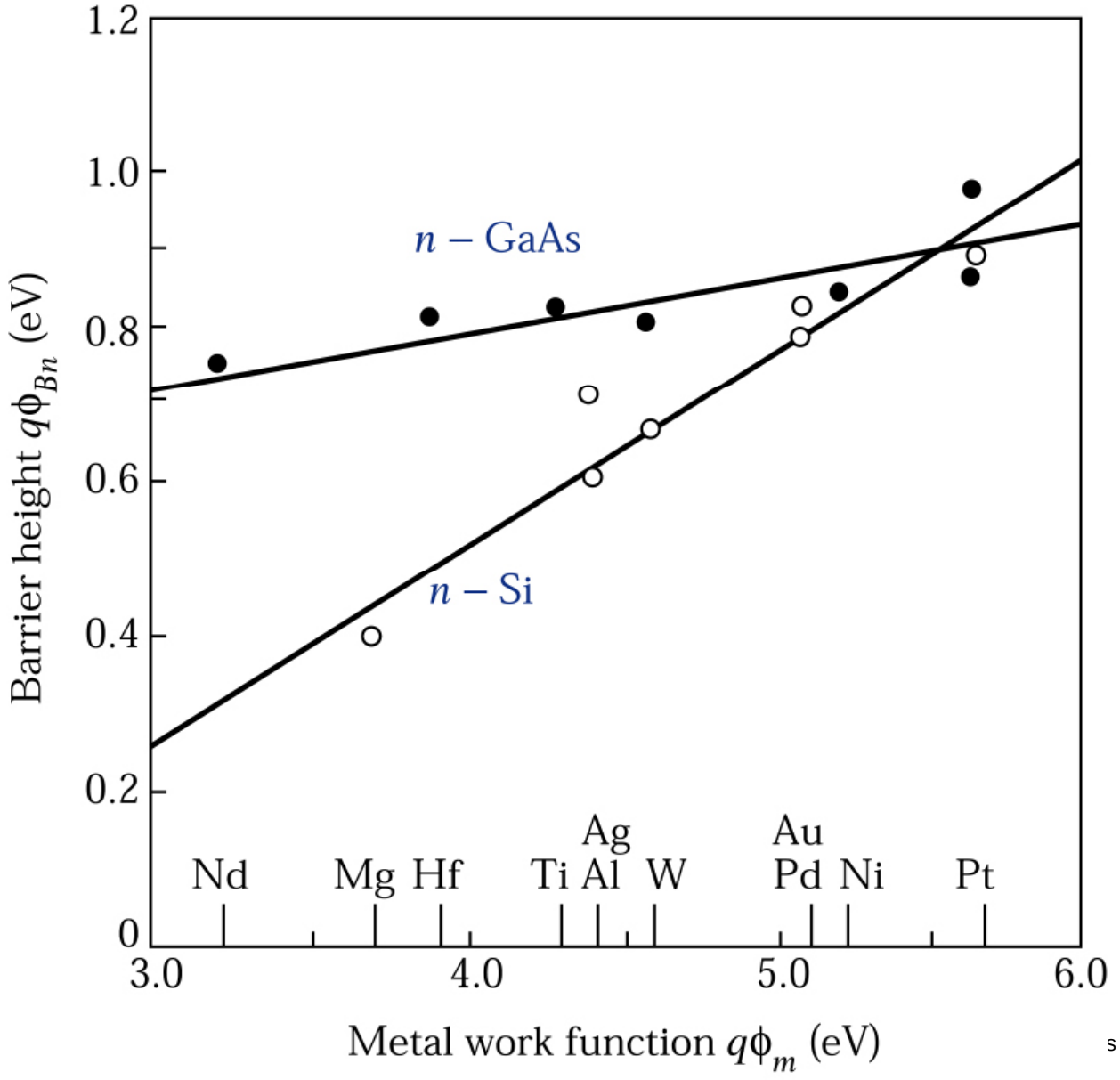
Energy band diagram of an isolated metal adjacent to an isolated* n*-type semiconductor



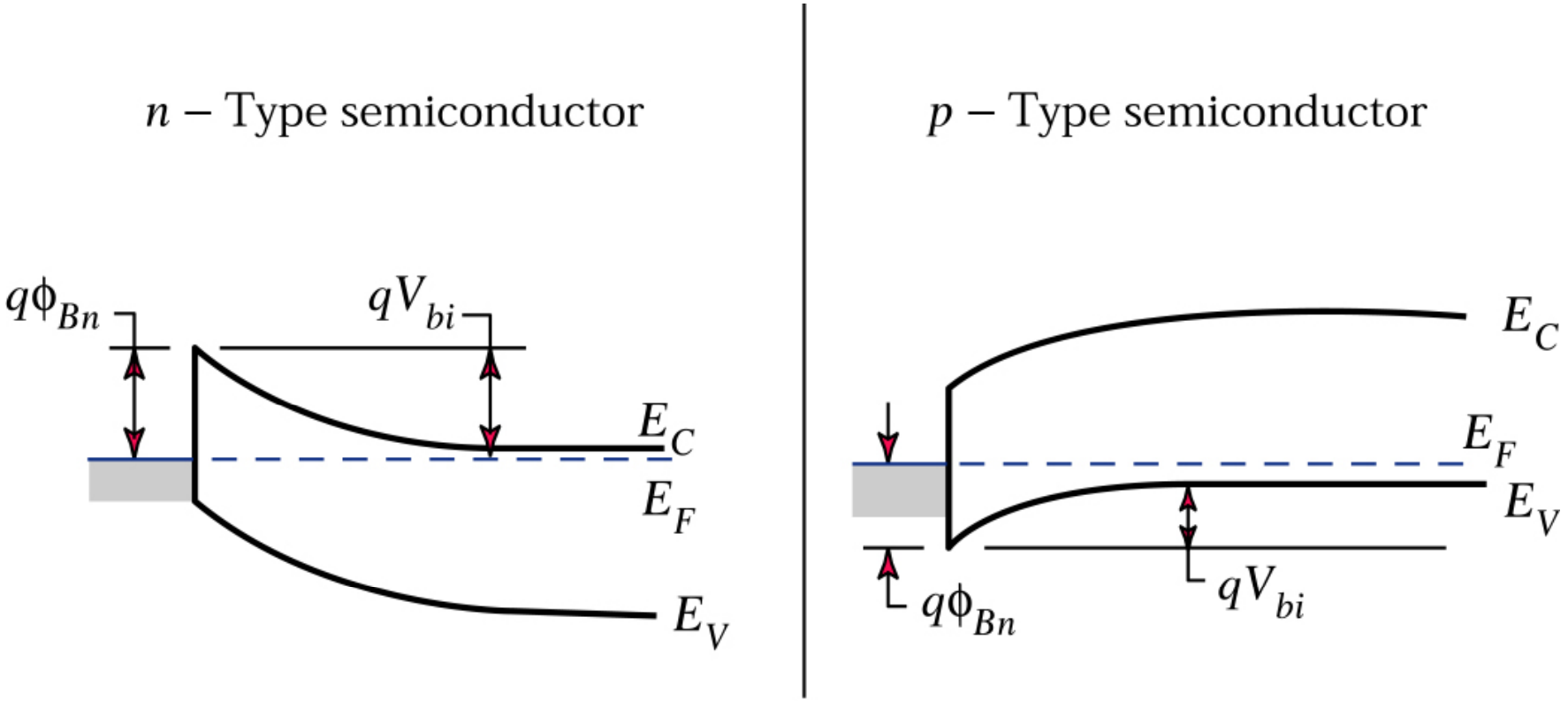
Energy band diagram of a metal-semiconductor contact in thermal equilibrium.



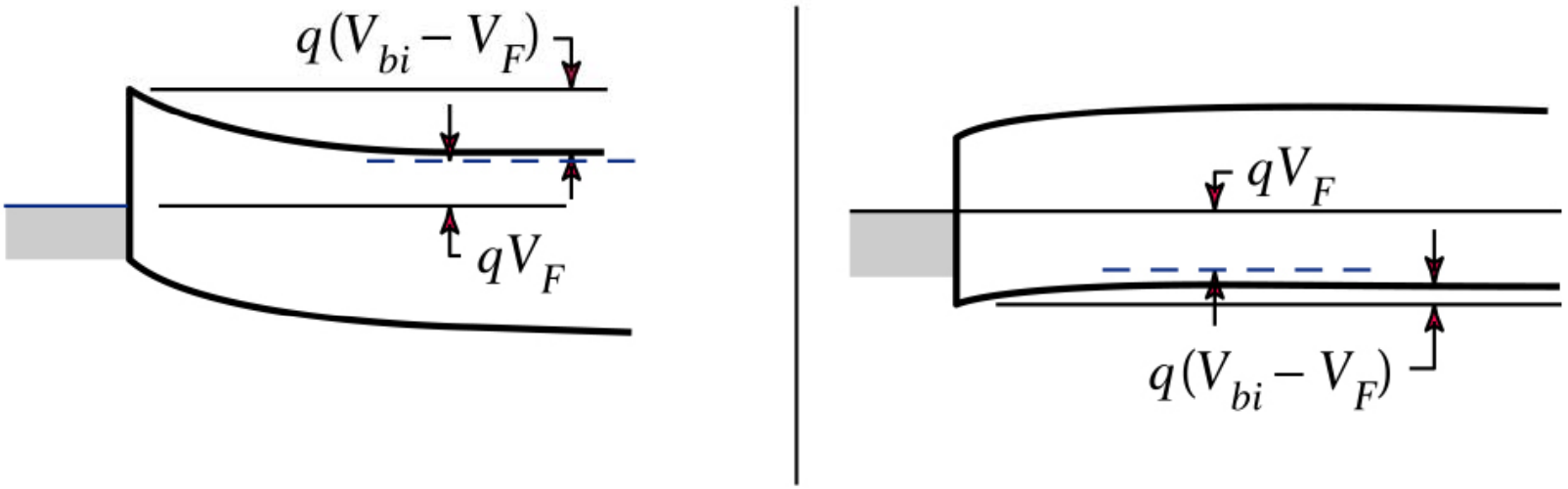
Measured barrier height for metal-silicon and metal-gallium arsenide contacts



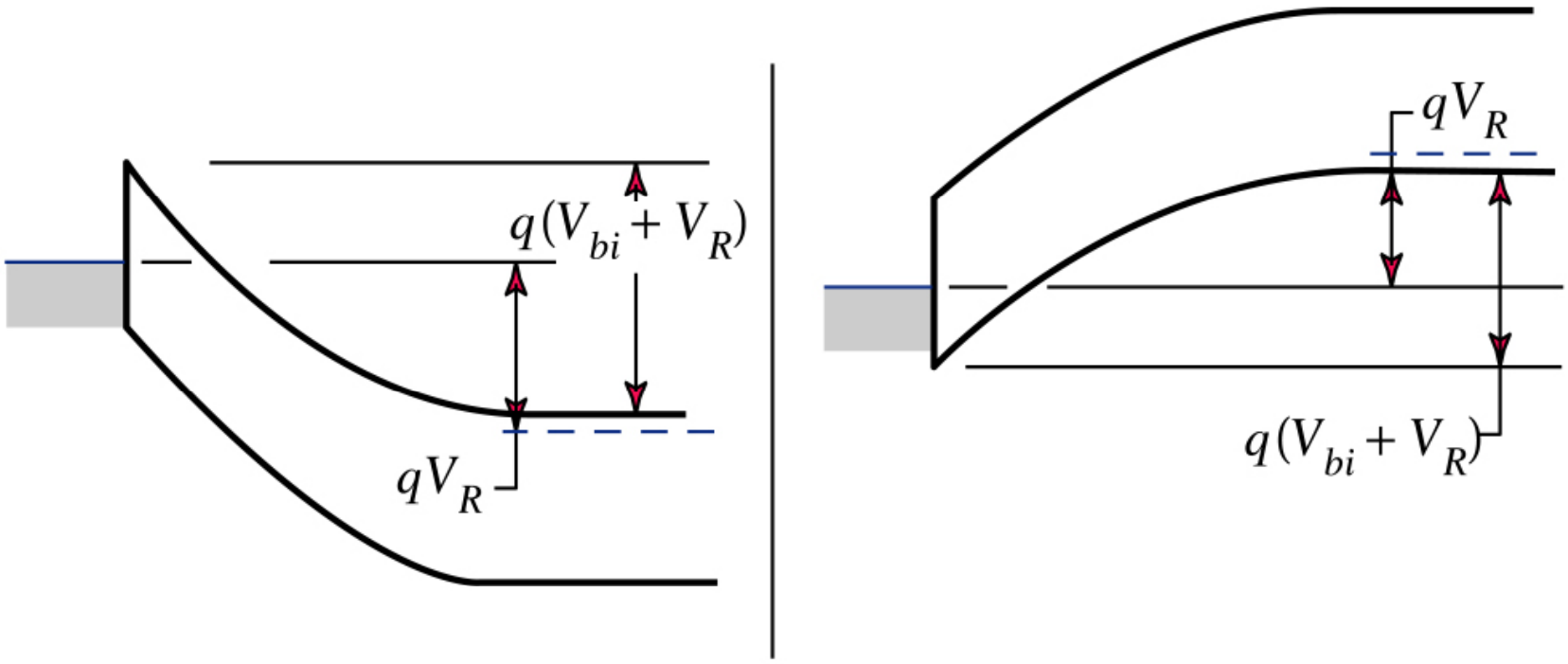
Energy band diagrams of metal
n-*type and* p-*type semiconductors under thermal equilibrium*



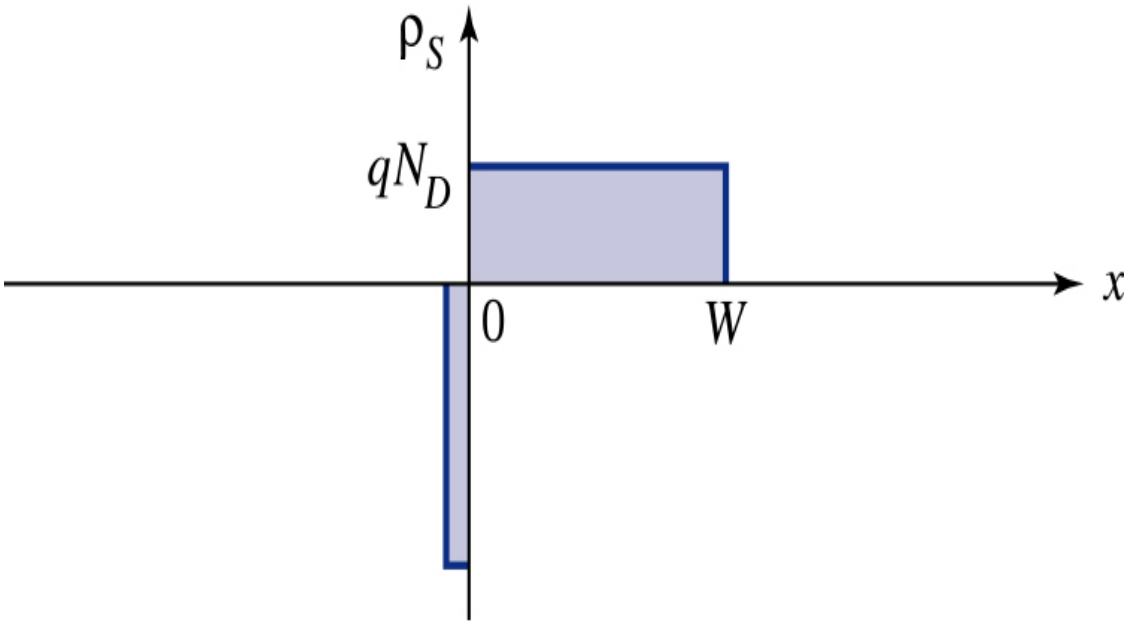
Energy band diagrams of metal n-*type and* p-*type semiconductors under forward bias*



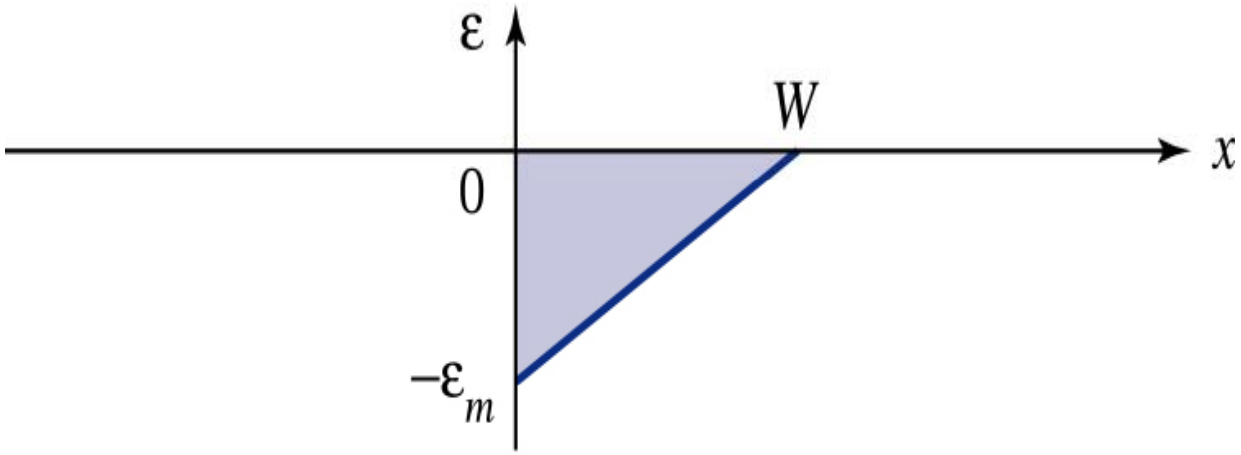
Energy band diagrams of metal
n-*type and* p-*type semiconductors under reverse bias.*



Charge distribution



electric-field distribution



Depletion Layer

$$\rho = -qN_D \qquad 0 < x < W$$

$$\nabla^2 V = \frac{\rho}{\varepsilon_s} = -\frac{qN_D}{\varepsilon_s}$$

$$\nabla E = \frac{dE}{dx} = -\frac{qN_D}{\varepsilon_s}$$

$$E(x) = \frac{qN_D}{\varepsilon_s}(W - x)$$

$$V_{bi} - V = \int_0^W E(x)dx = \frac{qN_D}{\varepsilon_s}\int_0^W (W - x)dx$$

$$= \frac{qN_D}{\varepsilon_s}\int_W^0 (W - x)d(W - x) = \frac{qN_D W^2}{2\varepsilon_s}$$

Depletion width

$$W = \sqrt{2\varepsilon_s (V_{bi} - V)/qN_D}$$

Charge per unit area

$$Q = QN_D W = \sqrt{2q\varepsilon_s N_D (V_{bi} - V)}$$

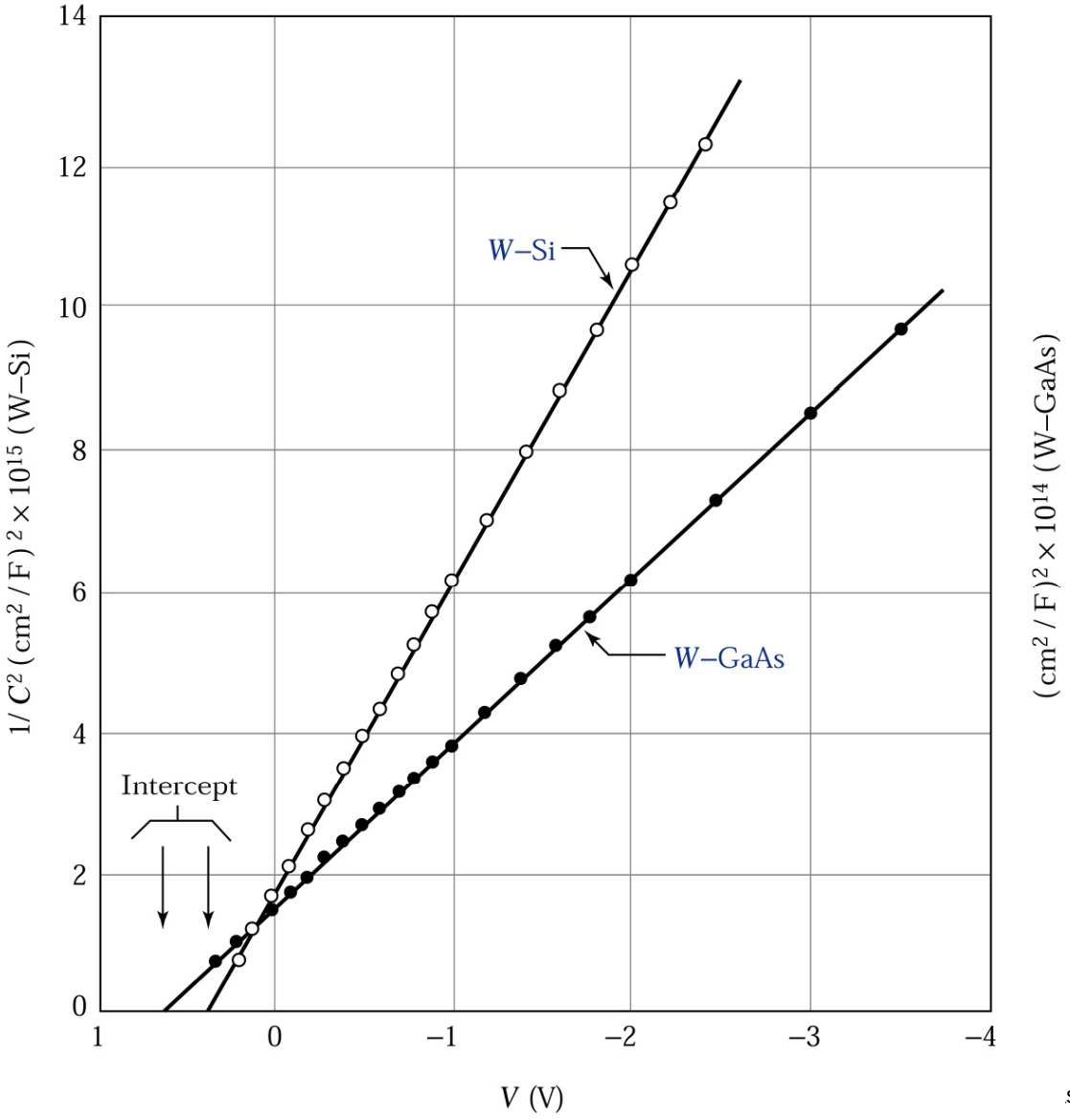
Capacitance

Per unit area: $$C = \frac{\partial Q}{\partial V} = \sqrt{\frac{q\varepsilon_s N_D}{2(V_{bi} - V)}} = \frac{\varepsilon_s}{W}$$

Rearranging: $$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\varepsilon_s N_D}$$

Or: $$N_D = \frac{2}{q\varepsilon_s}\left[\frac{-1}{d\left(1/C^2\right)/dV}\right]$$

1/C² versus applied voltage for W-Si and W-GaAs diodes



1/C² vs V

- If straight line – constant doping profile –

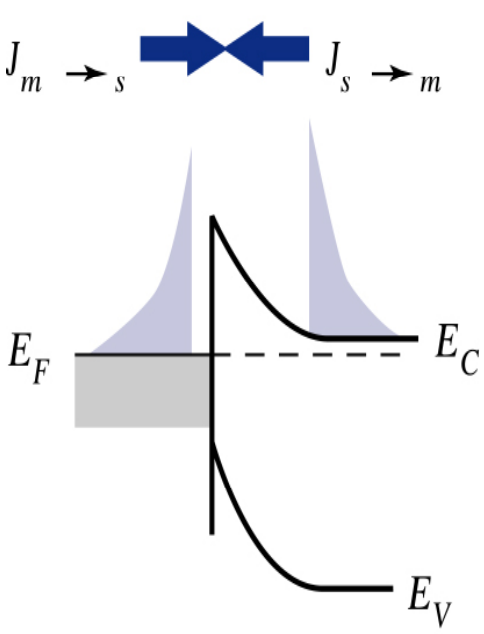
  slope = doping concentration

- If not straight line, can be used to find profile
- Intercept = V_{bi} can be used to find ϕ_{Bn}

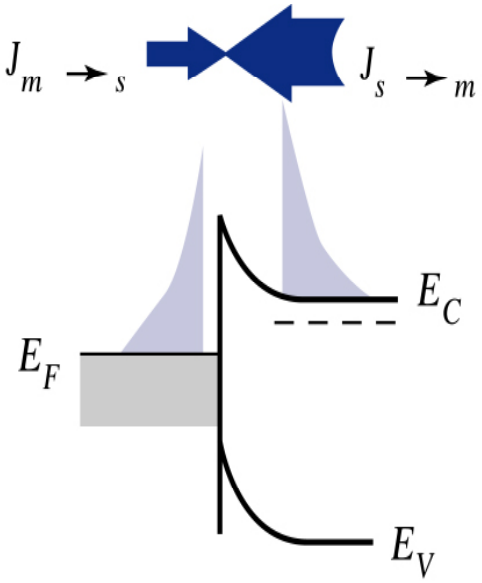
$$\phi_{Bn} = V_n + V_{bi}$$

$$V_n = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

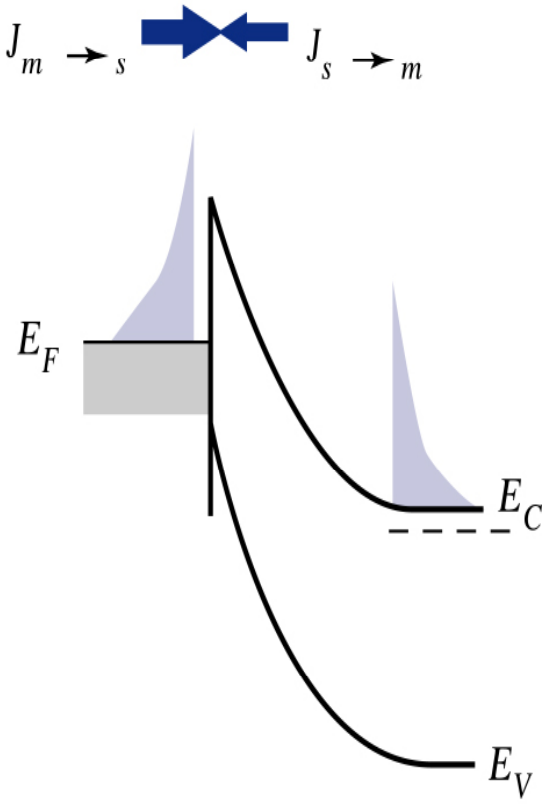
Current transport by the thermionic emission process



Thermal equilibrium



forward bias



reverse bias

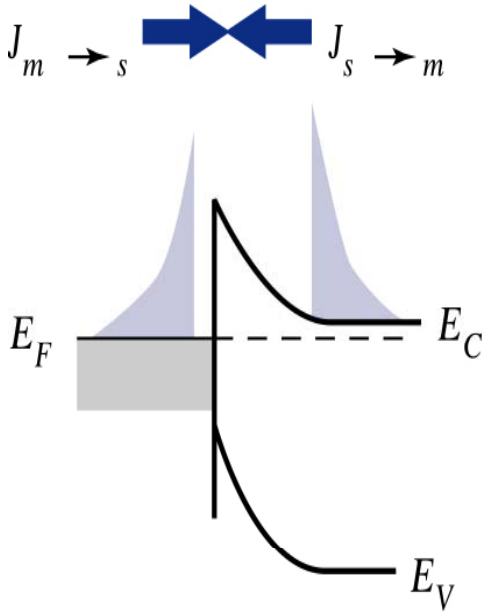
Thermionic emission

Number of electrons with enough thermal energy to overcome barrier:

$$n_{th} = N_C e^{\left(\frac{-q\phi_{Bn}}{kT}\right)}$$

At thermal equilibrium, current going both ways is the same:

$$\left|j_{m\to s}\right| = \left|j_{s\to m}\right| = C_1 N_C e^{\left(\frac{-q\phi_{Bn}}{kT}\right)}$$



Forward Bias

Barrier for electrons in semiconductor is reduced by V_F

$$n_{th} = N_C e^{\left(\frac{-(q\phi_{Bn} - V_F)}{kT}\right)}$$

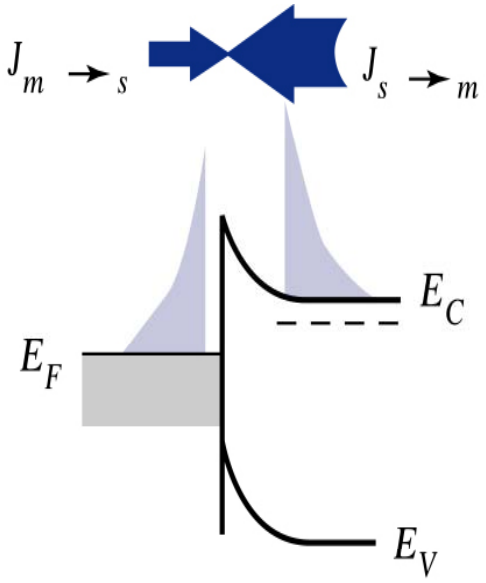
Barrier for electrons from metal to semiconductor is the same

Net current:

$$j = \left|j_{s\to m}\right| - \left|j_{m\to s}\right| = C_1 N_C e^{\left(\frac{-q(\phi_{Bn} - V_F)}{kT}\right)} - C_1 N_C e^{\left(\frac{-q\phi_{Bn}}{kT}\right)}$$

$$j = C_1 N_C e^{\left(\frac{-q\phi_{Bn}}{kT}\right)}\left(e^{\frac{qV_F}{kT}} - 1\right)$$

$$C_1 N_C = A^* T^2$$



Forward Bias

$$j = j_s\left(e^{\frac{qV}{kT}} - 1\right)$$

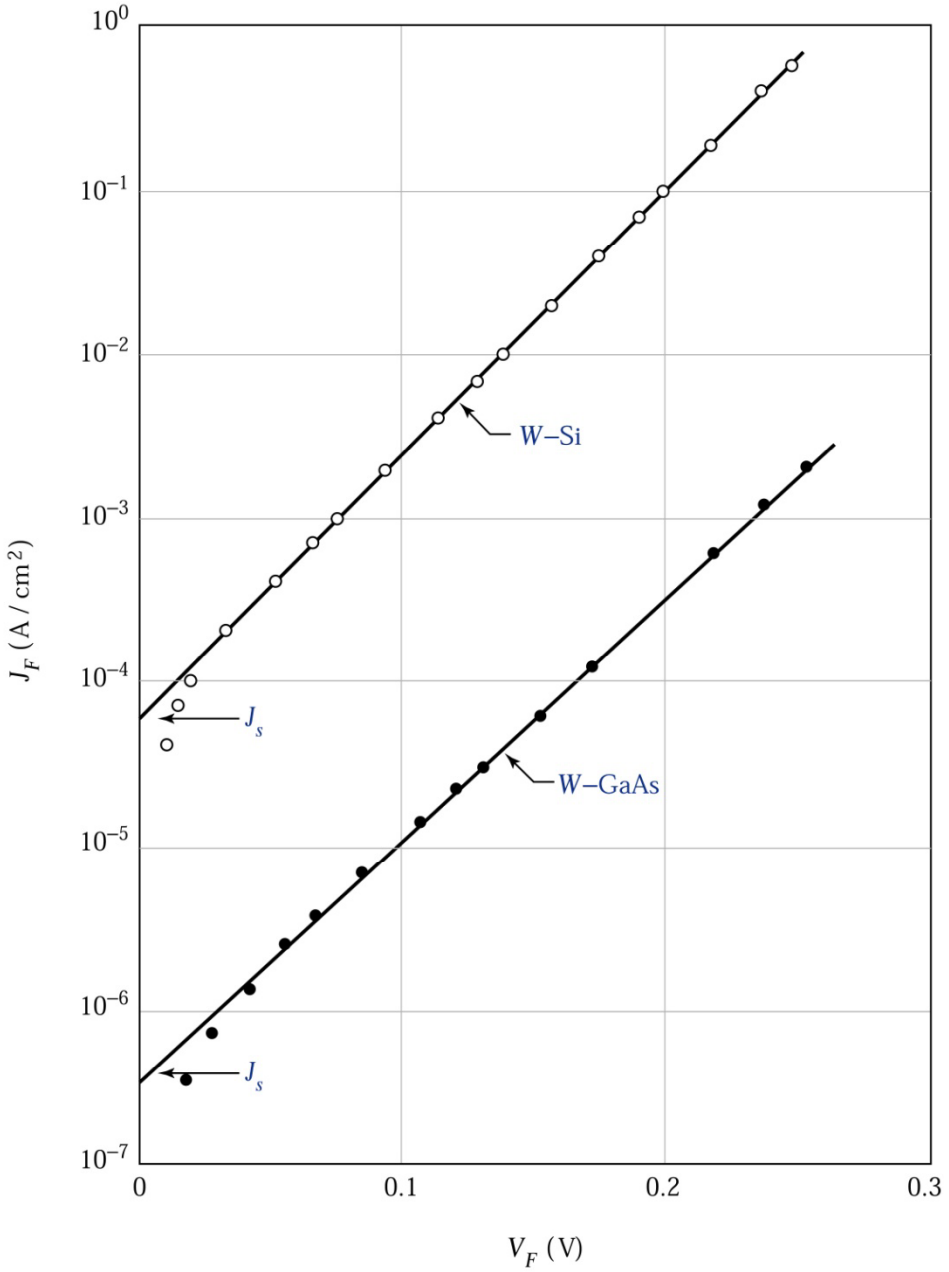
$$j_s = A^* T^2 e^{\frac{-q\phi_{Bn}}{kT}}$$

Effective Richardson Constant $$A^* = \frac{4\pi q m_e^* k^2}{h^3}$$

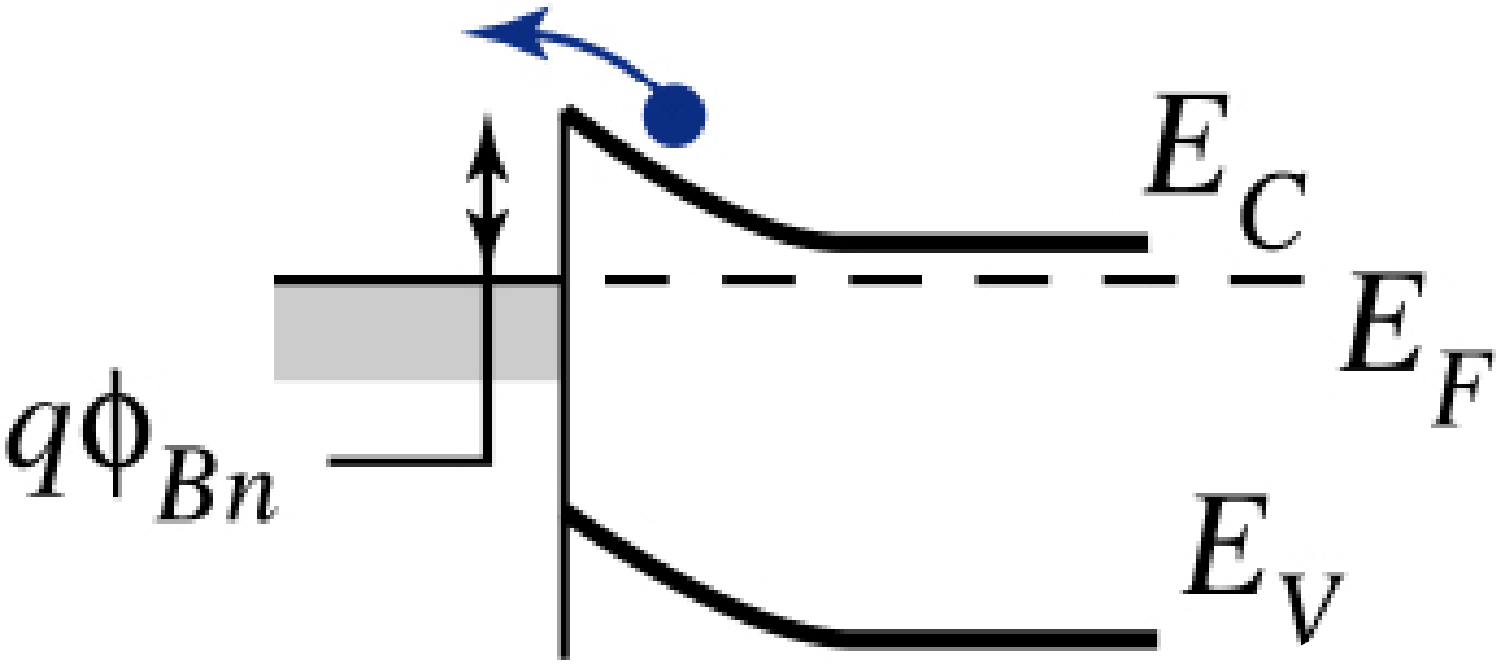
Derive by determining current with integral of velocity and density of states

$$j = \int v(E)dN(E) = \int v(E)g(E)f(E)dE$$

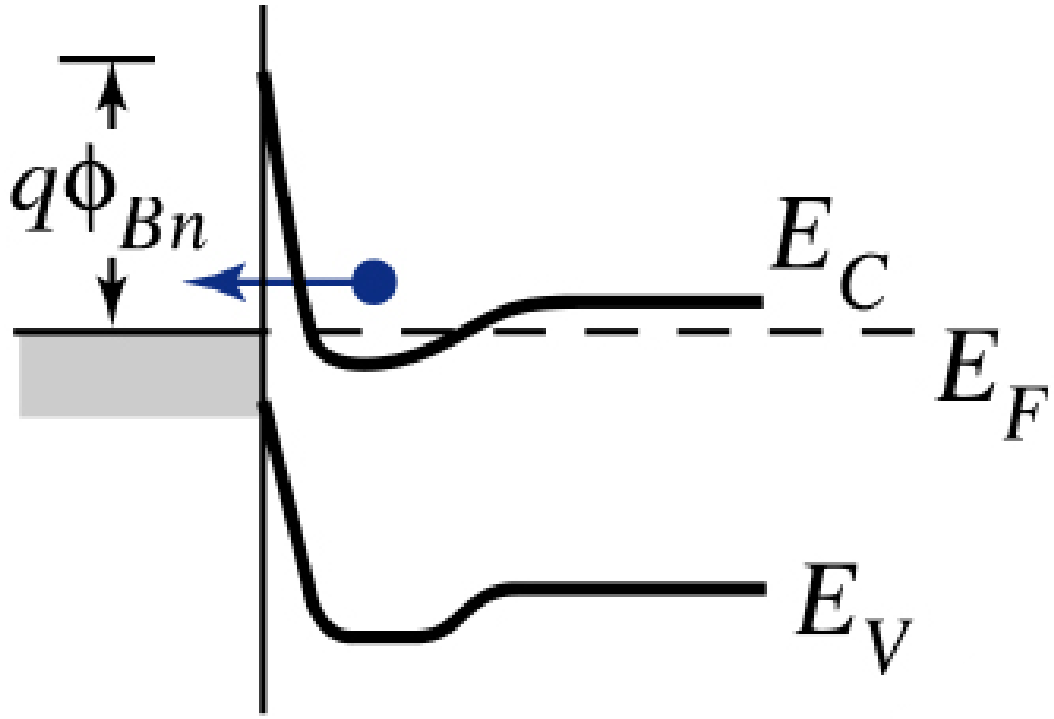
Forward current density vs applied voltage of W-Si and W-GaAs diodes



Thermionic Emission over the barrier – low doping



Tunneling through the barrier – high doping



Tunneling through the barrier

Narrow depletion width for high doping – tunneling

From QM 101:

Wavefunction is exponential depending on barrier width and height
probability of making it to the other side ~ ψ^2

$$\Psi(x,t) = e^{-i\omega t} e^{-\alpha x} \qquad \alpha = \sqrt{\frac{2m(U-E)}{\hbar^2}}$$

$$I \sim \exp\left[-2W\sqrt{2m(q\phi_{Bn} - qV)/\hbar^2}\right]$$

$$W = \sqrt{2\varepsilon_s (V_{bi} - V)/qN_D}$$

$$I \sim \exp\left[\frac{-C_2(\phi_{Bn} - V)}{\sqrt{N_D}}\right] \qquad C_2 = 4\sqrt{m\varepsilon_s}/\hbar$$

Contact resistance

Specific Contact Resistance(based on current density)

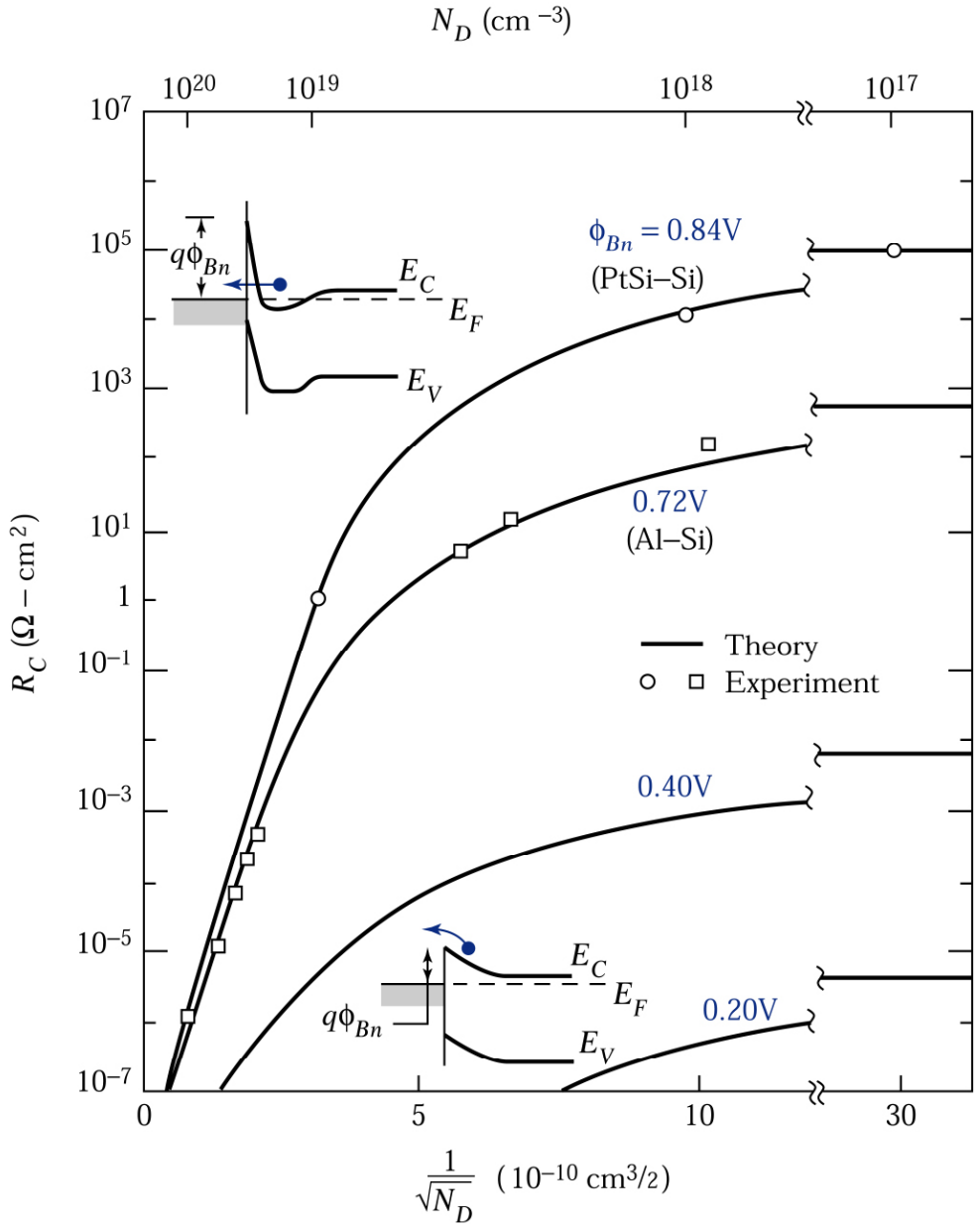
$$R_C \equiv \left(\frac{\partial J}{\partial V} \right)^{-1}_{V=0}$$

For tunneling current through barrier (high doping):

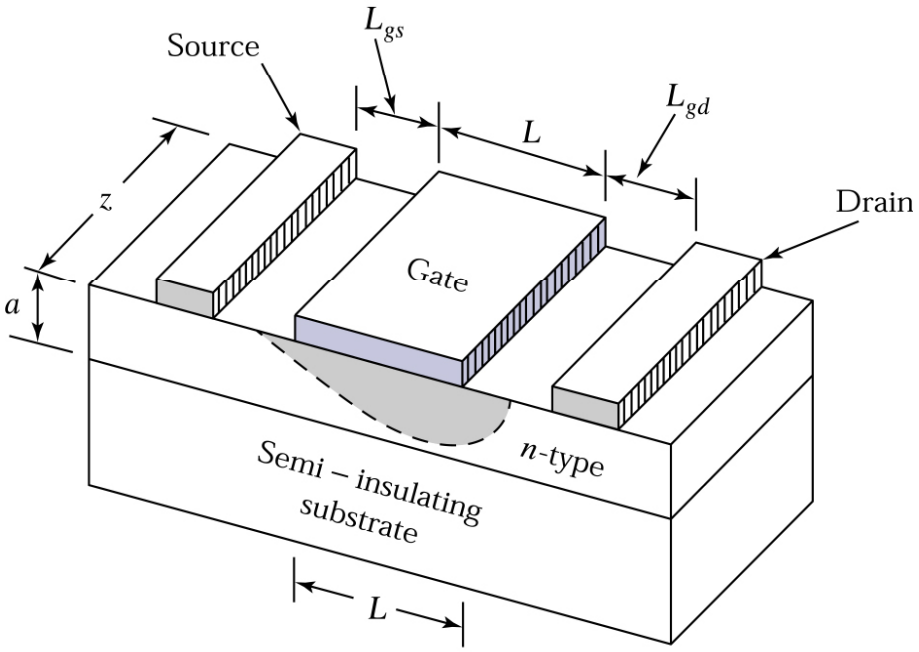
$$I \sim \exp\left[\frac{-C_2 \left(\phi_{Bn} - V \right)}{\sqrt{N_D}} \right]$$

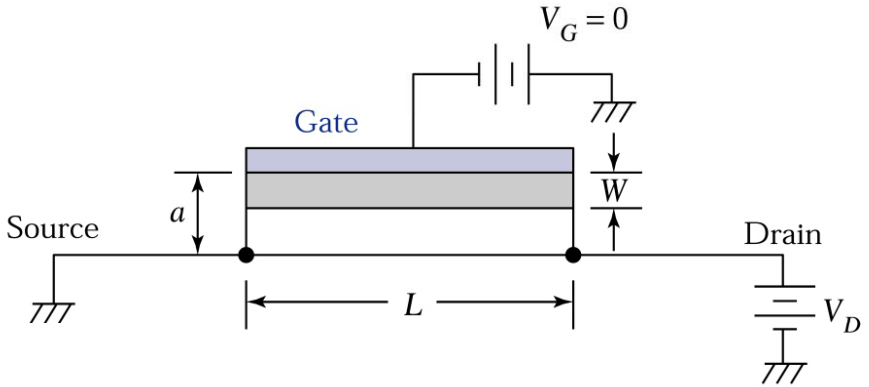
Ohmic Contact: $$R_C \sim \exp\left(\frac{C_2 \phi_{Bn}}{\sqrt{N_D}\hbar} \right)$$

Calculated and measured values of specific contact resistance

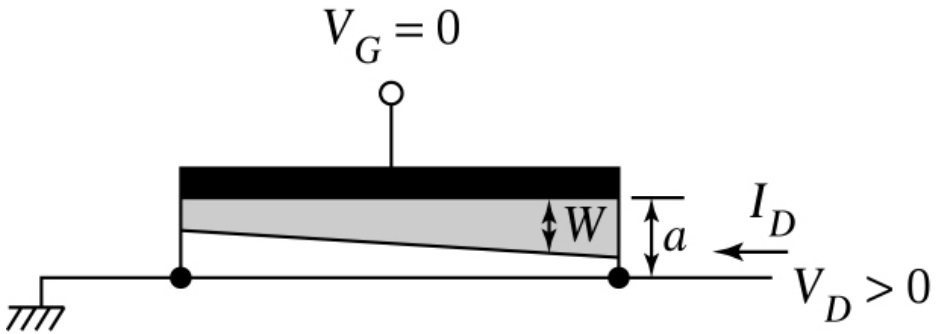


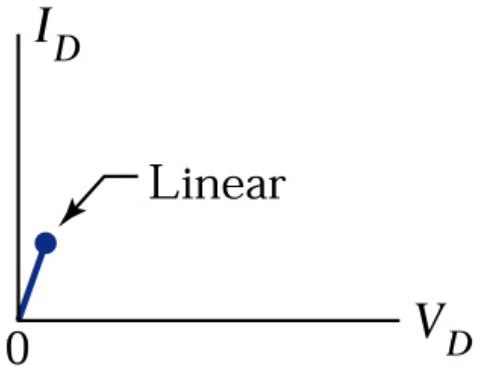
MESFET


Source
L_{gs}
L
L_{gd}
Drain
z
a
Gate
n-type
Semi – insulating
substrate
L


$V_G = 0$
Gate
W
a
Source
Drain
L
V_D

MESFET – Qualitative Operation

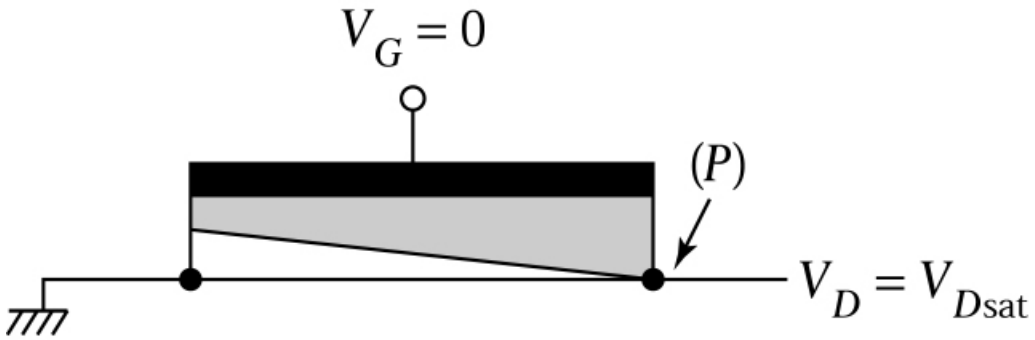


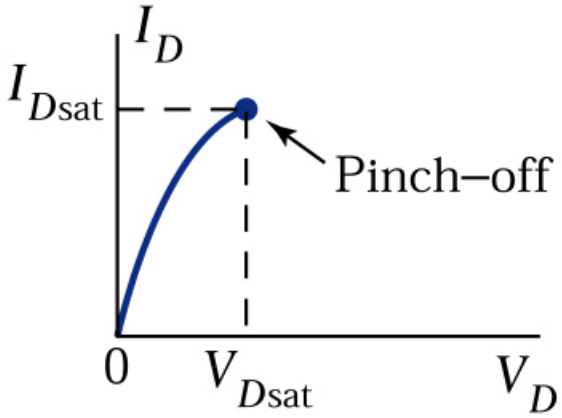


- No gate voltage – depletion from built-in voltage
- Positive drain voltage causes reverse bias
- Increased depletion width with increased V

$$R = \rho \frac{L}{A} = \frac{L}{q\mu_n N_D Z(a - W)}$$

MESFET – Qualitative Operation

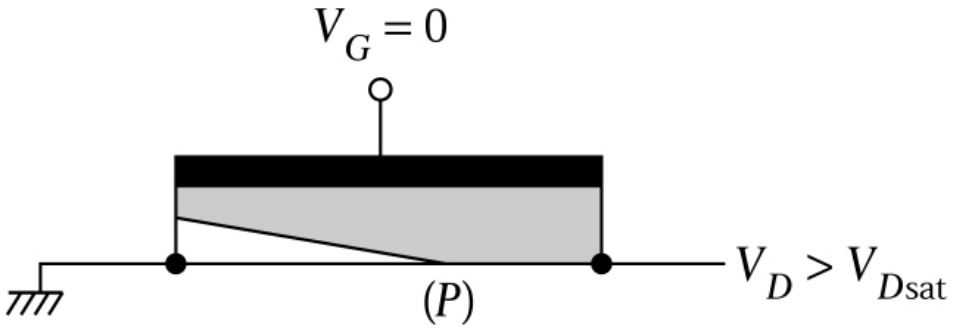


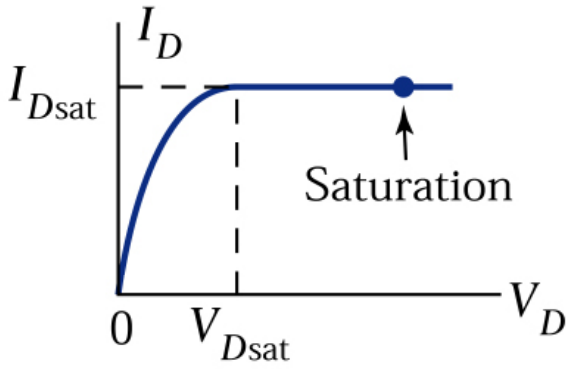


At higher drain voltages, W=a – pinch off at V_{Dsat}

$$V_{bi} - V = \frac{qN_D W^2}{2\varepsilon_s} \quad \Rightarrow \quad V_{Dsat} = \frac{qN_D a^2}{2\varepsilon_s} - V_{bi}$$

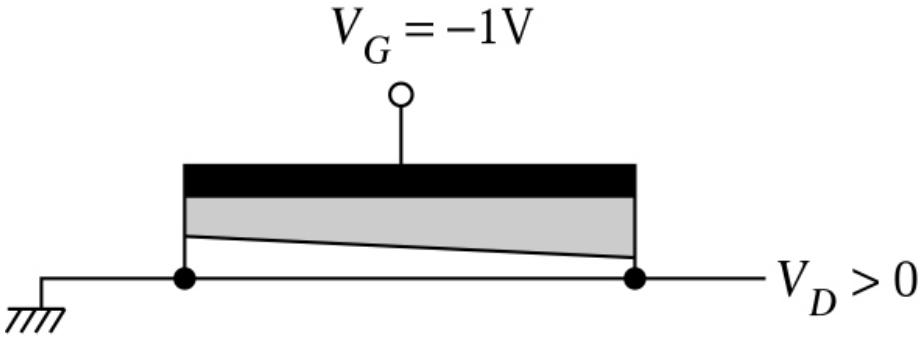
MESFET – Qualitative Operation

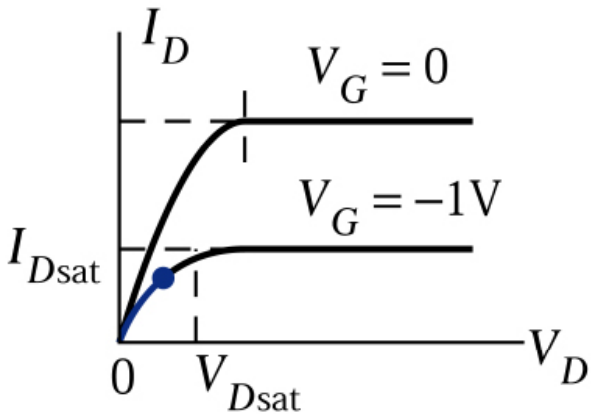




Above pinchoff voltage, drain current does not increase
Voltage at pinch-off point is still V_{dsat}

MESFET – Qualitative Operation

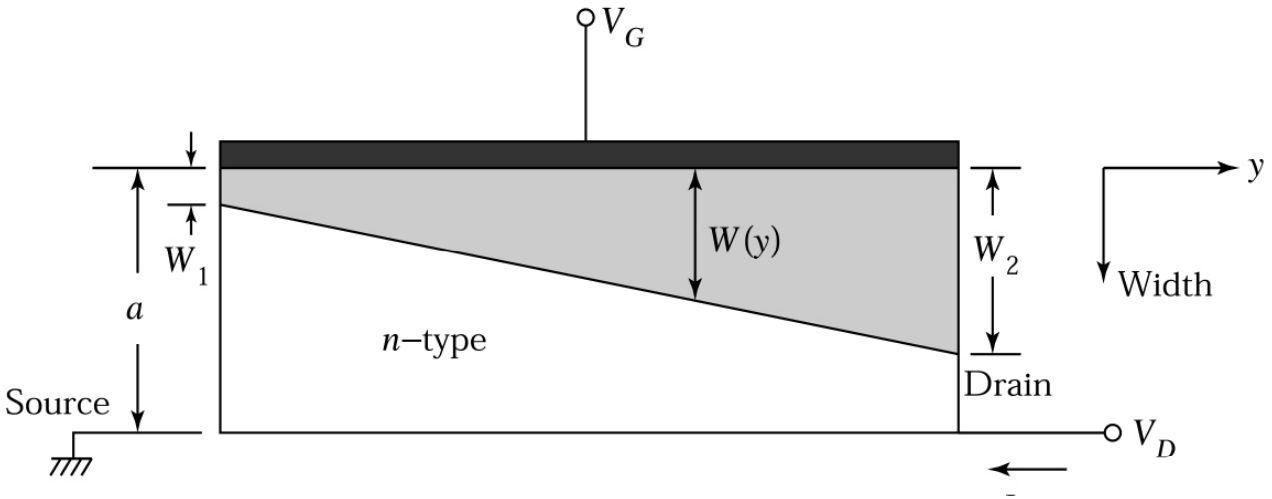




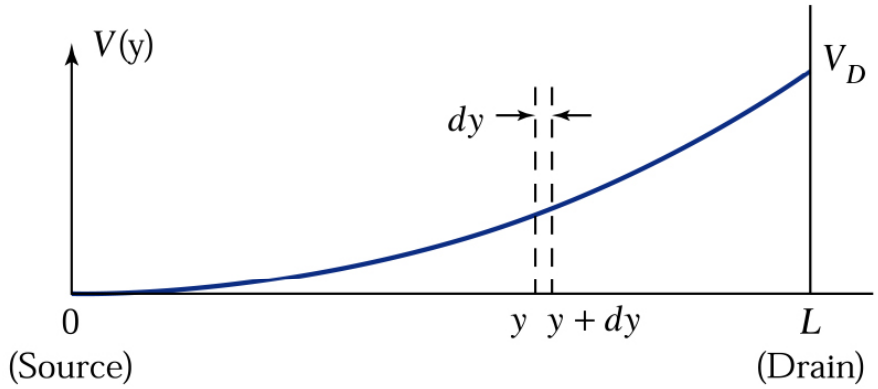
Addition of gate voltage (negative) increases baseline depletion width
Pinch-off occurs sooner
Saturation voltage and current are reduced (narrower channel)

$$V_{Dsat} = \frac{qN_D a^2}{2\varepsilon_s} - V_{bi} - V_G$$

I-V Characteristics – Linear Region



$$dV = I_D dR = \frac{I_D dy}{q\mu_n N_D Z[a - W(y)]}$$



$$W(y) = \sqrt{\frac{2\varepsilon_s\left(V(y) + V_G + V_{bi}\right)}{qN_D}}$$

$$dV = \frac{qN_D}{\varepsilon_s} W dW$$

I-V Characteristics – Linear Region

$$I_D dy = q\mu_n N_D Z\left[a - W(y)\right]dV$$

$$= q\mu_n N_D Z\left[a - W\right]\frac{qN_D}{\varepsilon_s} W dW$$

$$I_D = \frac{q^2 \mu_n N_D^2}{L\varepsilon_s}\int_{W_1}^{W_2}(a - W)W dW$$

$$I_D = \frac{q^2 \mu_n N_D^2}{2L\varepsilon_s}\left[a\left(W_2^2 - W_1^2\right) - \frac{2}{3}\left(W_2^3 - W_1^3\right)\right]$$

I-V Characteristics – Linear Region

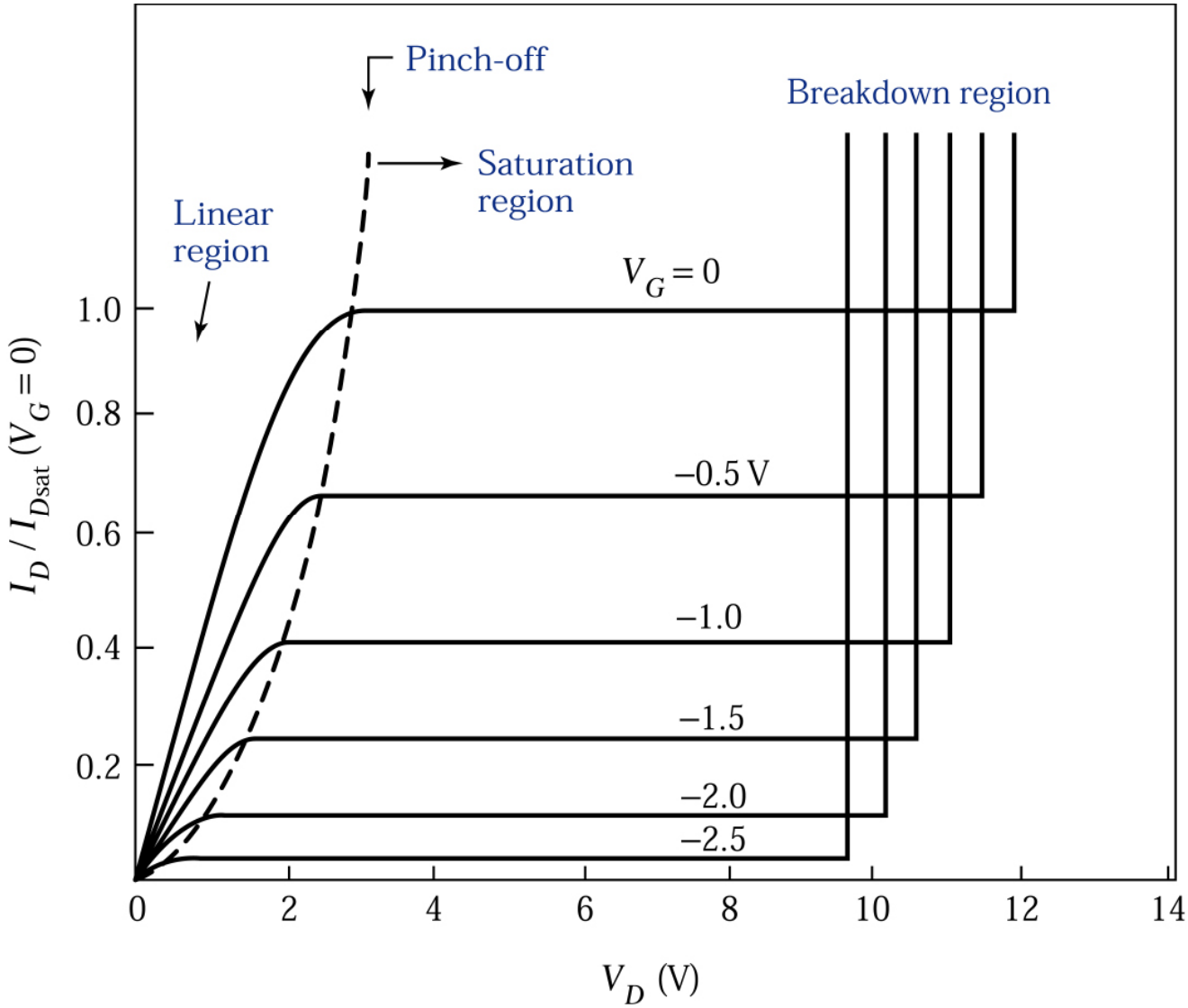
$$W_1 = \sqrt{\frac{2\varepsilon_s (V_G + V_{bi})}{qN_D}}$$

$$W_2 = \sqrt{\frac{2\varepsilon_s (V_D + V_G + V_{bi})}{qN_D}}$$

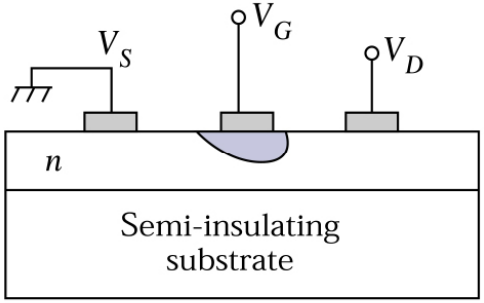
$$I_D = I_P \left[\frac{V_D}{V_P} - \frac{2}{3}\left(\frac{V_D + V_G + V_{bi}}{V_P} \right)^{3/2} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P} \right)^{3/2} \right]$$

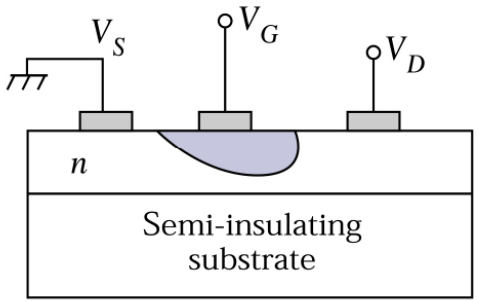
$$I_P \equiv \frac{Z\mu_n q^2 N_D^2 a^3}{2\varepsilon_s L}$$

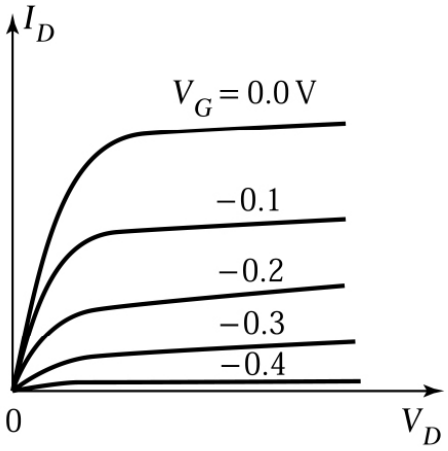
$$V_P \equiv \frac{qN_D a^2}{2\varepsilon_s}$$

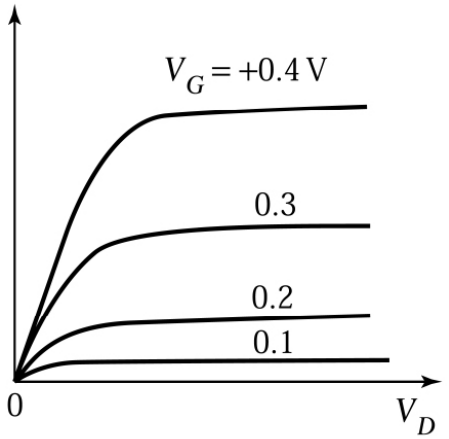


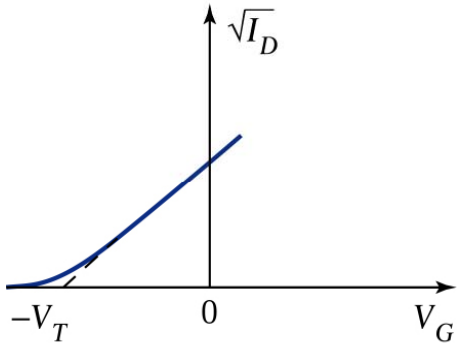
Normalized ideal current-voltage characteristics of a MESFET with V_P = 3.2 V.

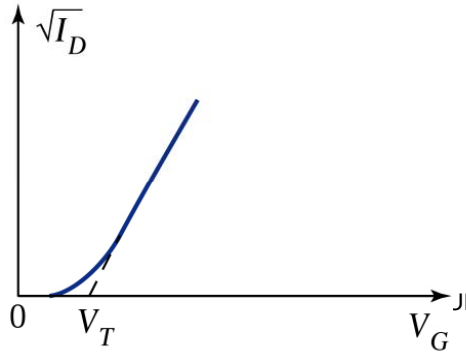

V_S
V_G
V_D
n
Semi-insulating substrate


V_S
V_G
V_D
n
Semi-insulating substrate


I_D
$V_G = 0.0$ V
−0.1
−0.2
−0.3
−0.4
0
V_D


$V_G = +0.4$ V
0.3
0.2
0.1
0
V_D


$\sqrt{I_D}$
$-V_T$
0
V_G


$\sqrt{I_D}$
0
V_T
V_G

Transconductance

$$I_D = I_P\left[\frac{V_D}{V_P} - \frac{2}{3}\left(\frac{V_D + V_G + V_{bi}}{V_P}\right)^{3/2} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P}\right)^{3/2}\right]$$

In Saturation: $V_P = V_D + V_G + V_{bi} \quad \Rightarrow \quad V_{Dsat} = V_P - V_G - V_{bi}$

$$I_{Dsat} = I_P\left[\frac{V_P - V_G - V_{bi}}{V_P} - \frac{2}{3}\left(\frac{V_P - V_G - V_{bi} + V_G + V_{bi}}{V_P}\right)^{3/2} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P}\right)^{3/2}\right]$$

$$I_{Dsat} = I_P\left[1 - \frac{(V_G + V_{bi})}{V_P} - \frac{2}{3} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P}\right)^{3/2}\right]$$

$$I_{Dsat} = I_P\left[\frac{1}{3} - \frac{(V_G + V_{bi})}{V_P} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P}\right)^{3/2}\right]$$

Transconductance

$$I_{Dsat} = I_P\left[\frac{1}{3} - \frac{(V_G + V_{bi})}{V_P} + \frac{2}{3}\left(\frac{V_G + V_{bi}}{V_P}\right)^{3/2}\right]$$

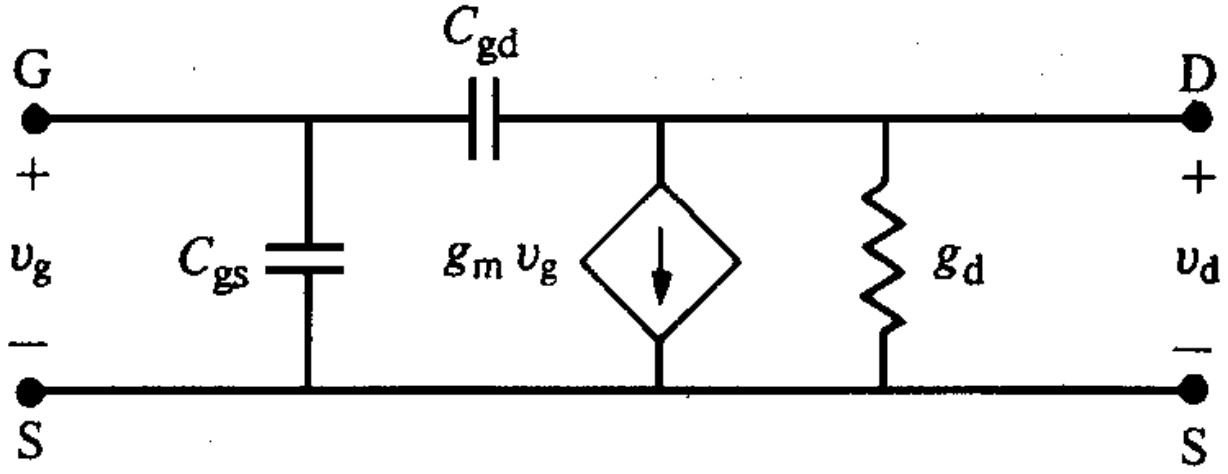
$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D}$$

$$g_m = I_P\left[0 - \frac{1}{V_P} + \frac{2}{3} * \frac{3}{2}(V_P)^{-3/2}(V_G + V_{bi})^{1/2}\right]$$

$$g_m = \frac{I_P}{V_P}\left(1 - \sqrt{\frac{V_G + V_{bi}}{V_P}}\right)$$

$$g_m = \frac{2Z\mu_n qN_D a}{L}\left(1 - \sqrt{\frac{V_G + V_{bi}}{V_P}}\right)$$

Equivalent Circuit - High Frequency AC



- Input stage looks like capacitances gate-to-channel
- Output capacitances ignored -drain-to-source capacitance small

Maximum Frequency (not in saturation)

- C_i is capacitance per unit area and C_{gate} is total capacitance of the gate

$$C_{gate} = C_i ZL$$

- $F=f_{max}$ when gain=1 ($i_{out}/i_{in}=1$)

$$f_{\max} = \frac{g_m}{2\pi C_{gate}}$$

$$C_{gate} = ZL\left(\frac{\varepsilon_S}{W}\right)$$

$$f_{\max} \approx \frac{\frac{2Z\mu_n qN_D a}{L}}{2\pi ZL\left(\frac{\varepsilon_S}{W}\right)} = \frac{\mu_n qN_D a^2}{2\pi L^2 \varepsilon_s}$$

Velocity Saturation

Drain current:

$$I_D = A * qn\upsilon_s = Z(a - W)qN_D\upsilon_s$$

Transconductance

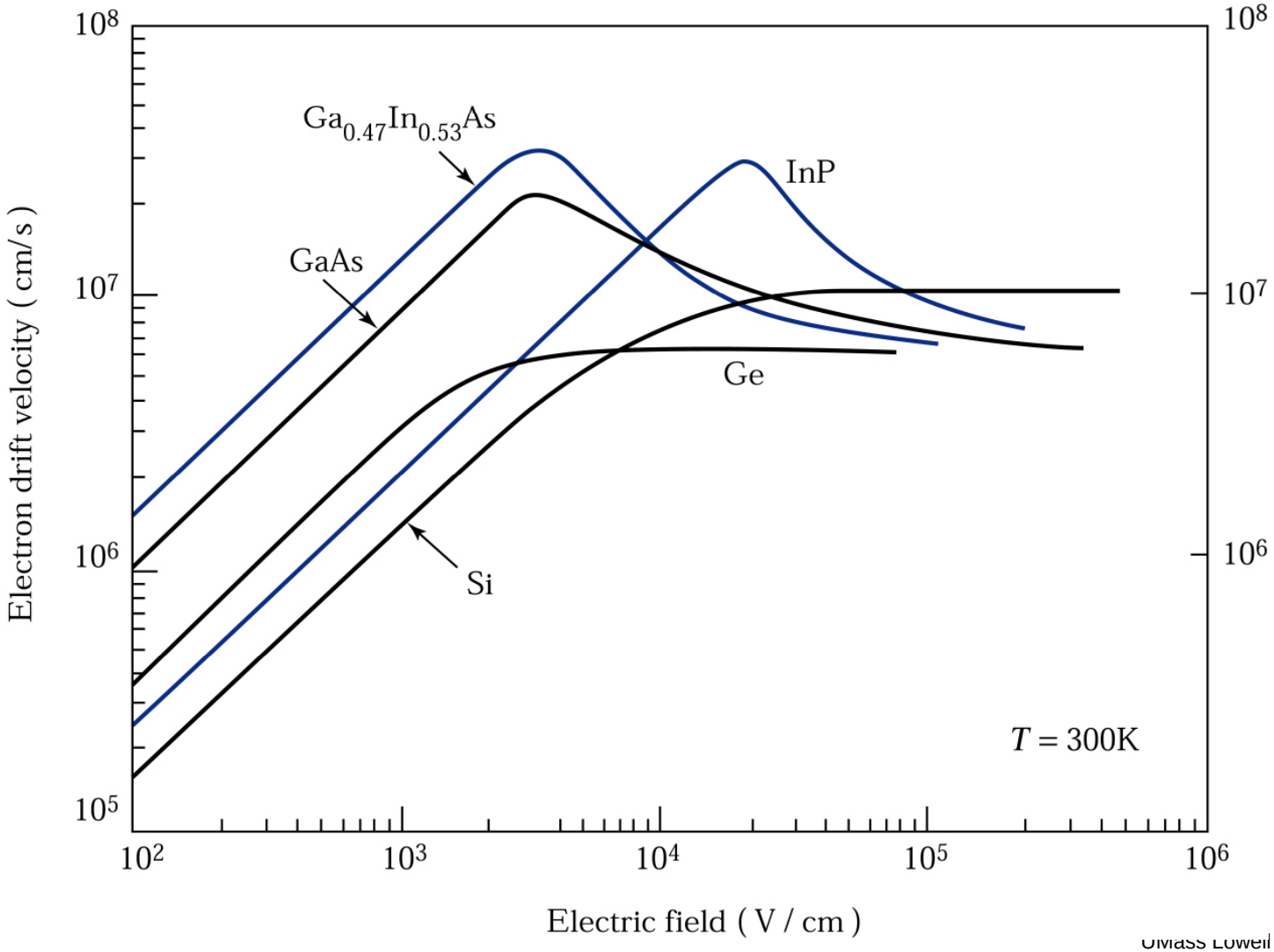
$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{\partial I_D}{\partial W}\frac{\partial W}{\partial V_G} = \frac{Z\upsilon_s\varepsilon_s}{W}$$

Cutoff Frequency:

$$f_{\max} = \frac{g_m}{2\pi C_{gate}}$$

$$f_{\max} = \frac{Z\upsilon_s\varepsilon_s / W}{2\pi ZL(\varepsilon_s / W)} = \frac{\varepsilon_S}{2\pi L}$$

Figure 7.15. ***The drift velocity versus the electric field for electrons in various semiconductor materials.***



III-V MESFETs – GaAs and InP

+Semi-insulating material – high speed devices (like built-in SOI)

+High Electron Mobility/Saturation Velocity – high speed

+Direct Bandgap – photonic devices

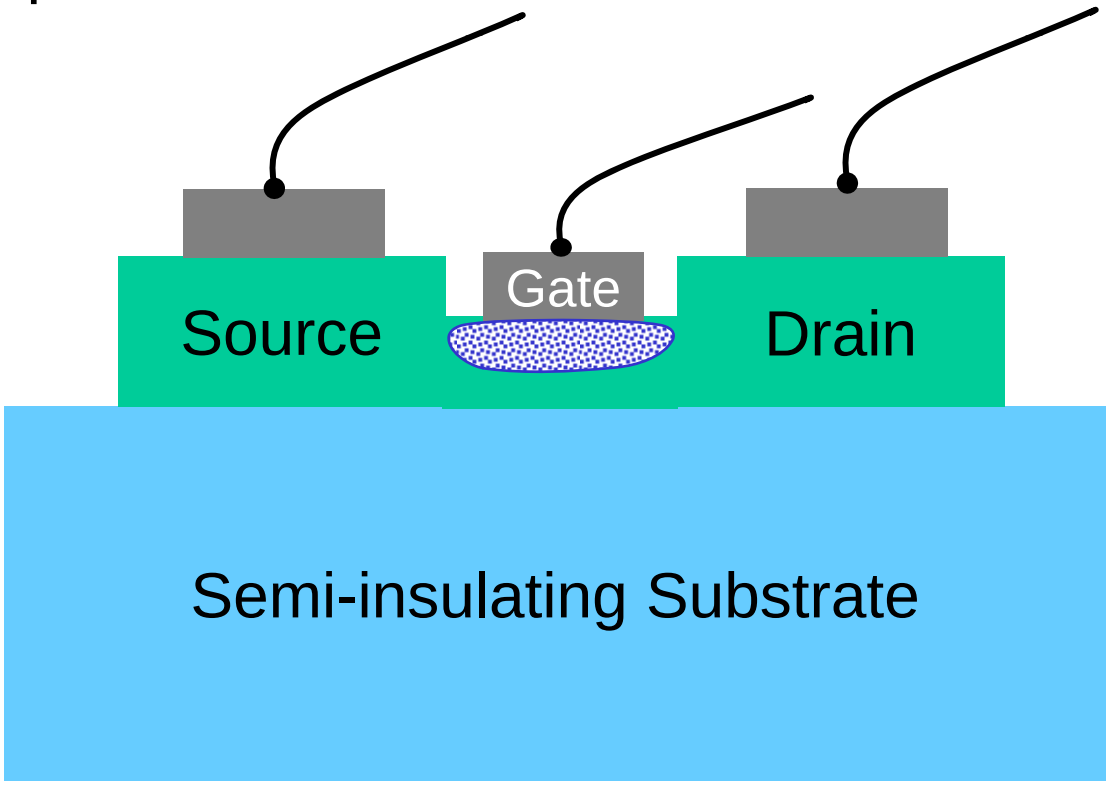
+Heterostructures – bandgap engineering

-No Simple Oxides – MOSFETS not viable – no equivalent to SiO_2

III-V Transistors: GaAs

No simple oxides for GOX – MOSFETS not widely used

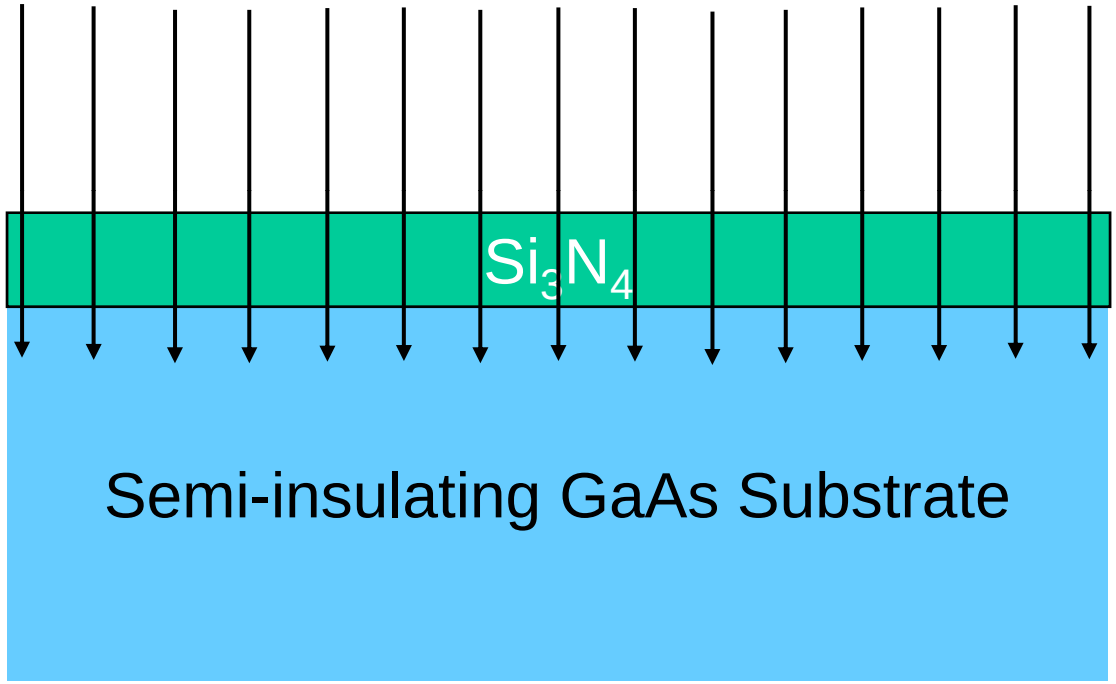
MESFET structure more common – mesa structure depletion mode transistor



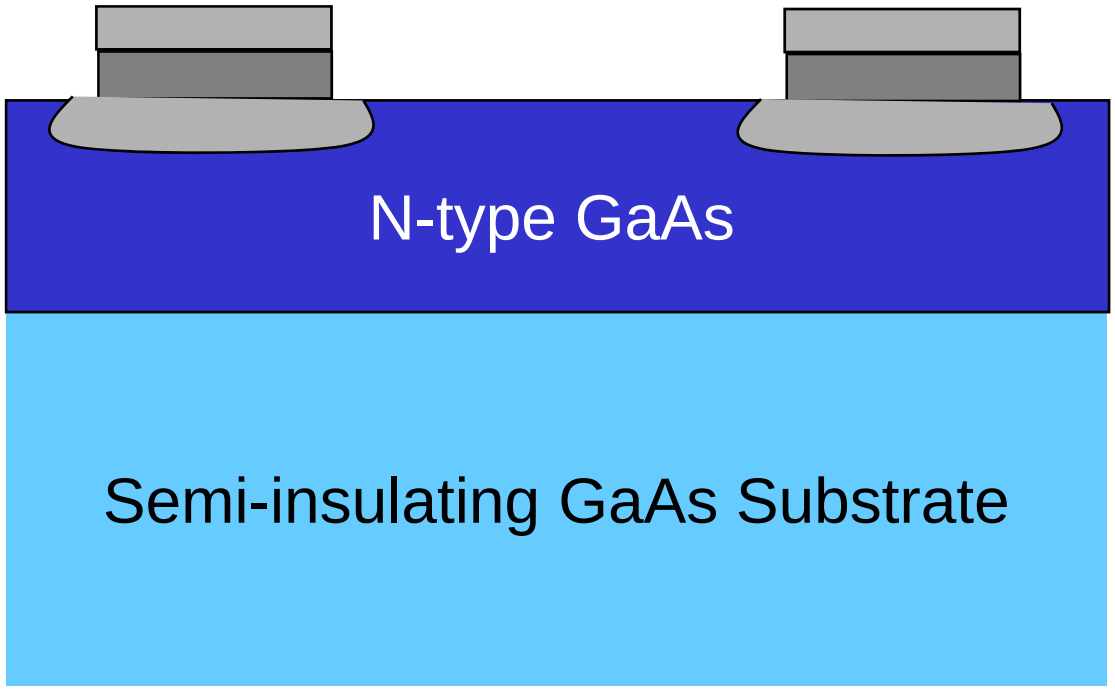
Depletion Mode GaAs MESFET

- N-type material – high electron mobility
- Mesa etch for isolation on SI substrate
- Ohmic contacts for Source and Drain – alloyed
- Shottky contact for Gate – Ti
- Recessed gate – depth determines threshold

GaAs MESFET Fabrication

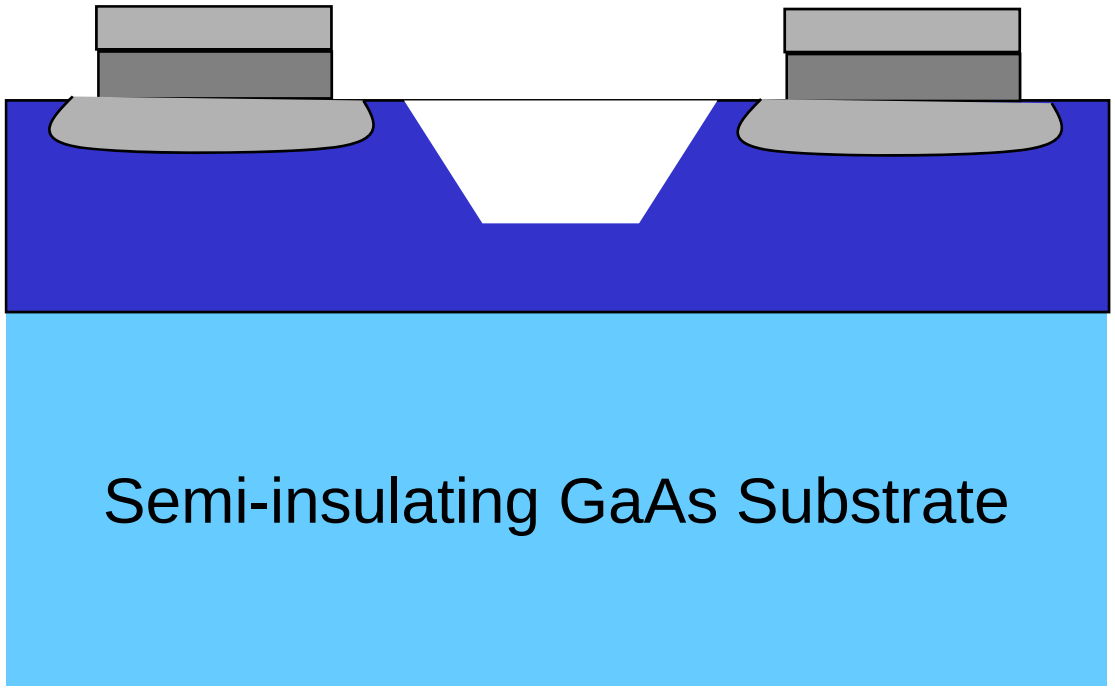


Deposit Si_3N_4 layer, implant Si and anneal for form n-type material
Can also grow n-type epi layer by MBE or MOCVD



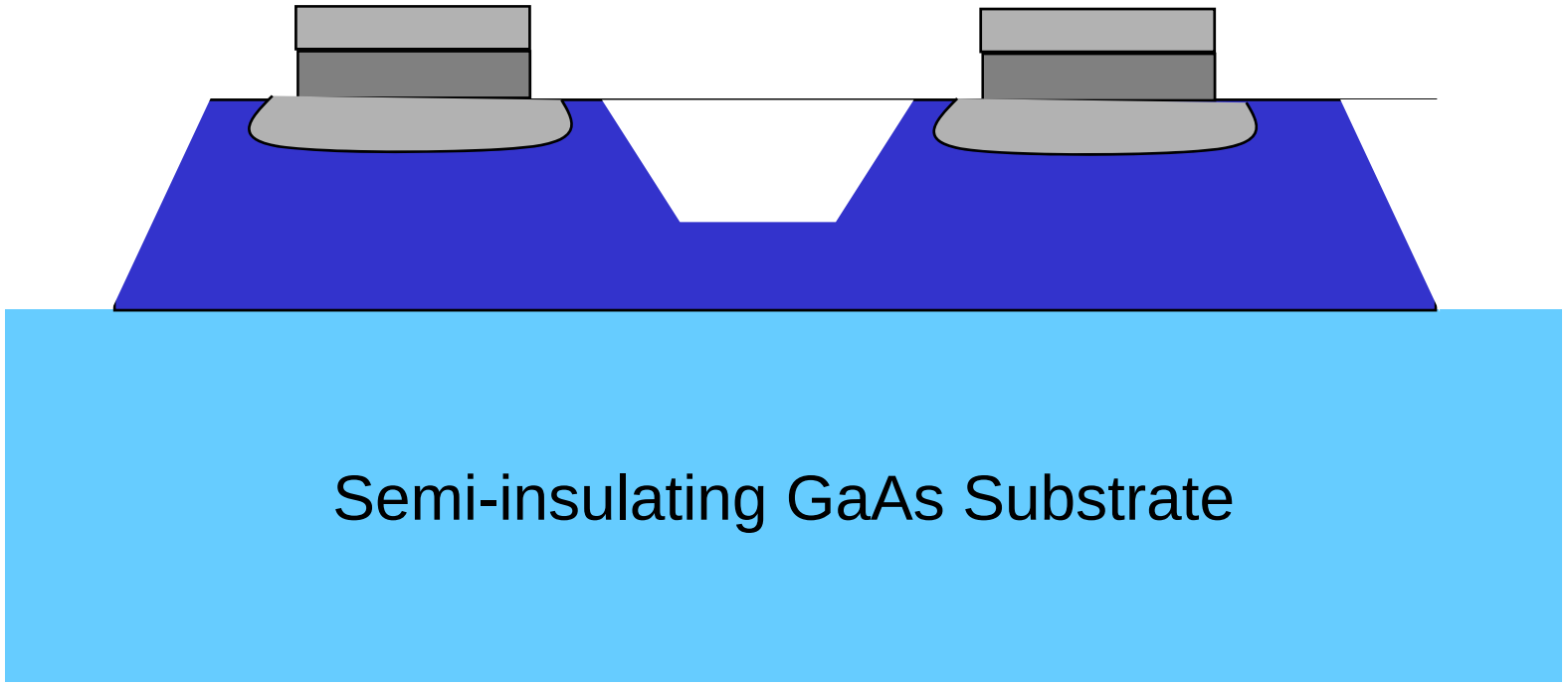
Ohmic contact formation for source and drain – NiAuGe

evaporate Au(88wt%)Ge(12wt%) then Ni (+Au)
anneal 30 min at 450°C in H_2/N_2
Au reacts with Ga from substrate – Ga vacancies
Ge fills Ga vacancies – heavy n-type doping
low contact resistance ohmic
Ge doping not uniform – spreading resistance effect



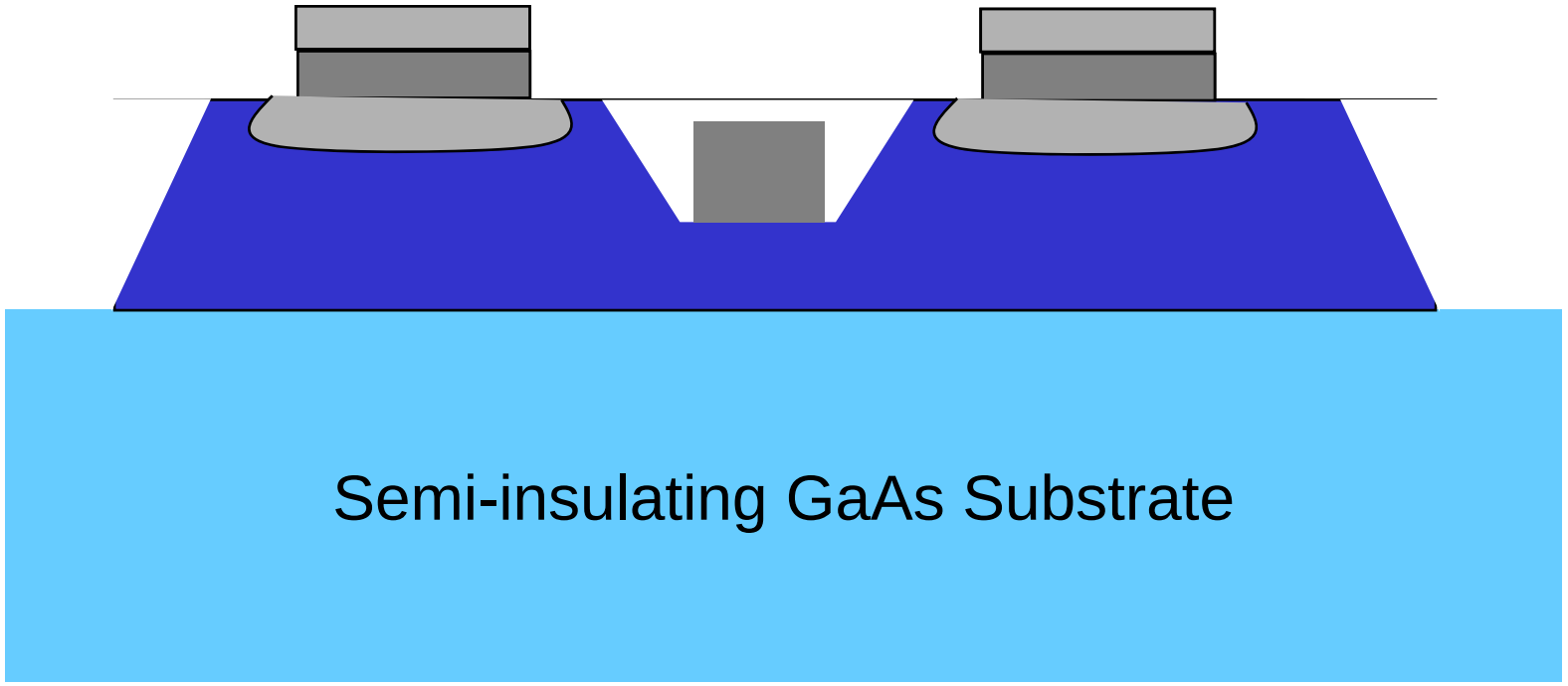
Gate Recess Etch

Wet etching
Channel depth determines pinch-off voltage
Channel resistance can be monitored *in-situ*



Mesa Recess Etch

Wet etching
Semi-insulating substrate for device isolation



Shottky Gate Electrode deposition – Ti/Pt/Au or Ti/Pd/Au

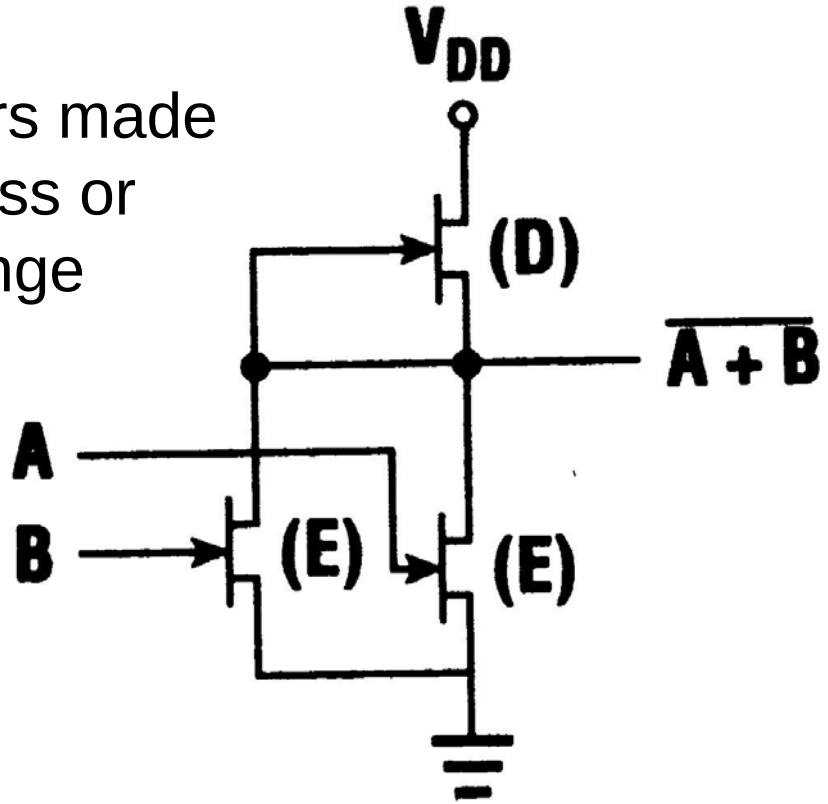
Almost any metal will form barrier
Ga diffuses in many metals
Ti –contact
Pt or Pd barrier layer
Au added for low resistivity

GaAs Digital Circuits:

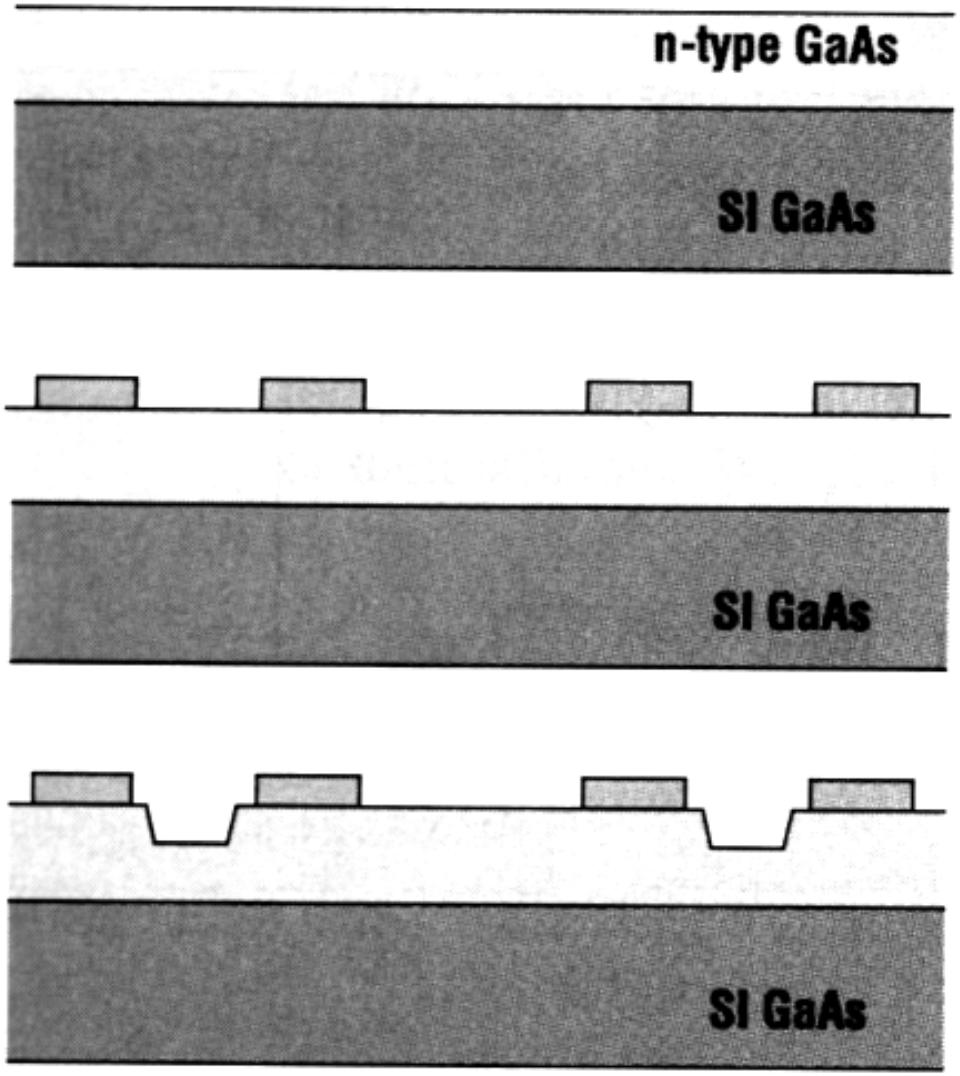
Direct Coupled FET Logic (DCFL) – lowest power and highest level of integration

Uses enhancement and depletion mode transistors

Enhancement mode transistors made using thinner gate recess or different doping to change threshold



DCFL Fabrication Sequence

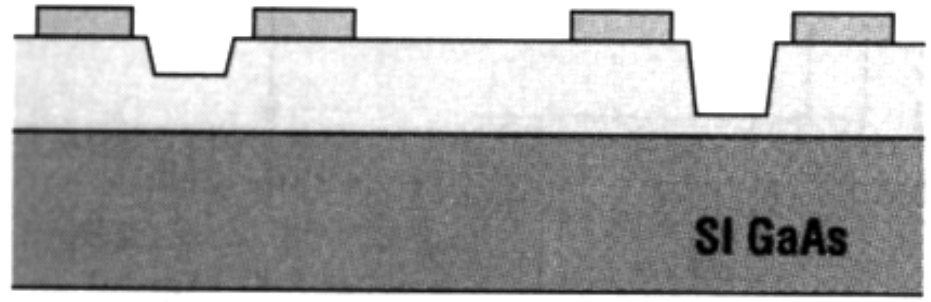


Step 1- Epitaxial growth

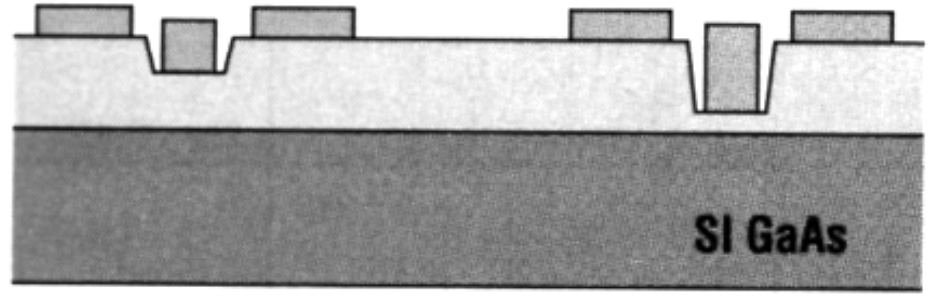
Step 2- Ohmic contact

Step 3- Gate recess

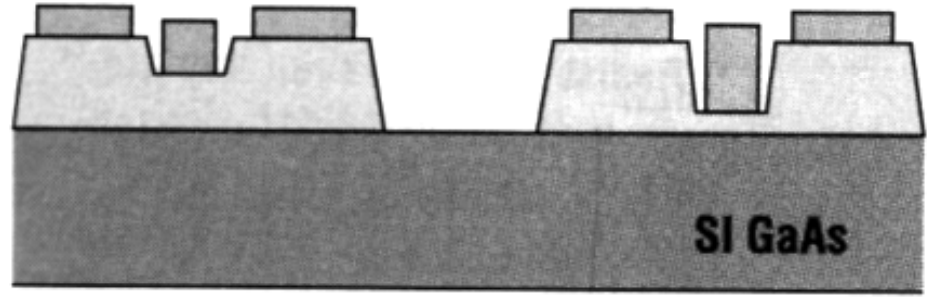
DCFL Fabrication Sequence(cont.)



Step 4- e-mode recess



Step 5- Gate Schottky



Step 6- Meso etch